

Compal Confidential

A4WAZ/A4WAR Schematics Document

AMD "Carrizo/Carrizo-L" Platform

AMD 12~25W APU With Excavator/Puma+ Core and 25W DGPU with Meso/Exo

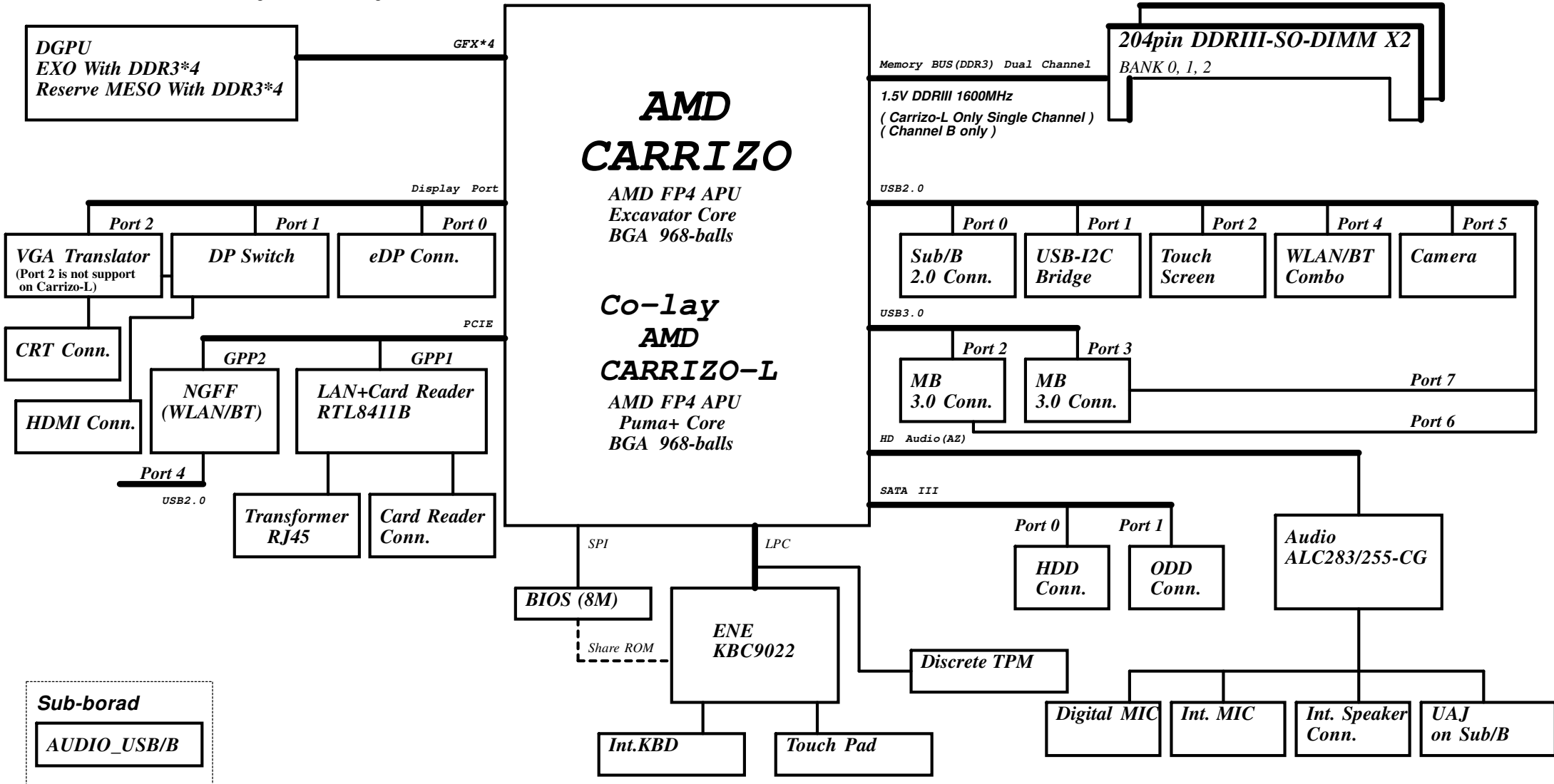
LA-C351PR01 REV:1A

2015-02-26

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				Size	Document Number
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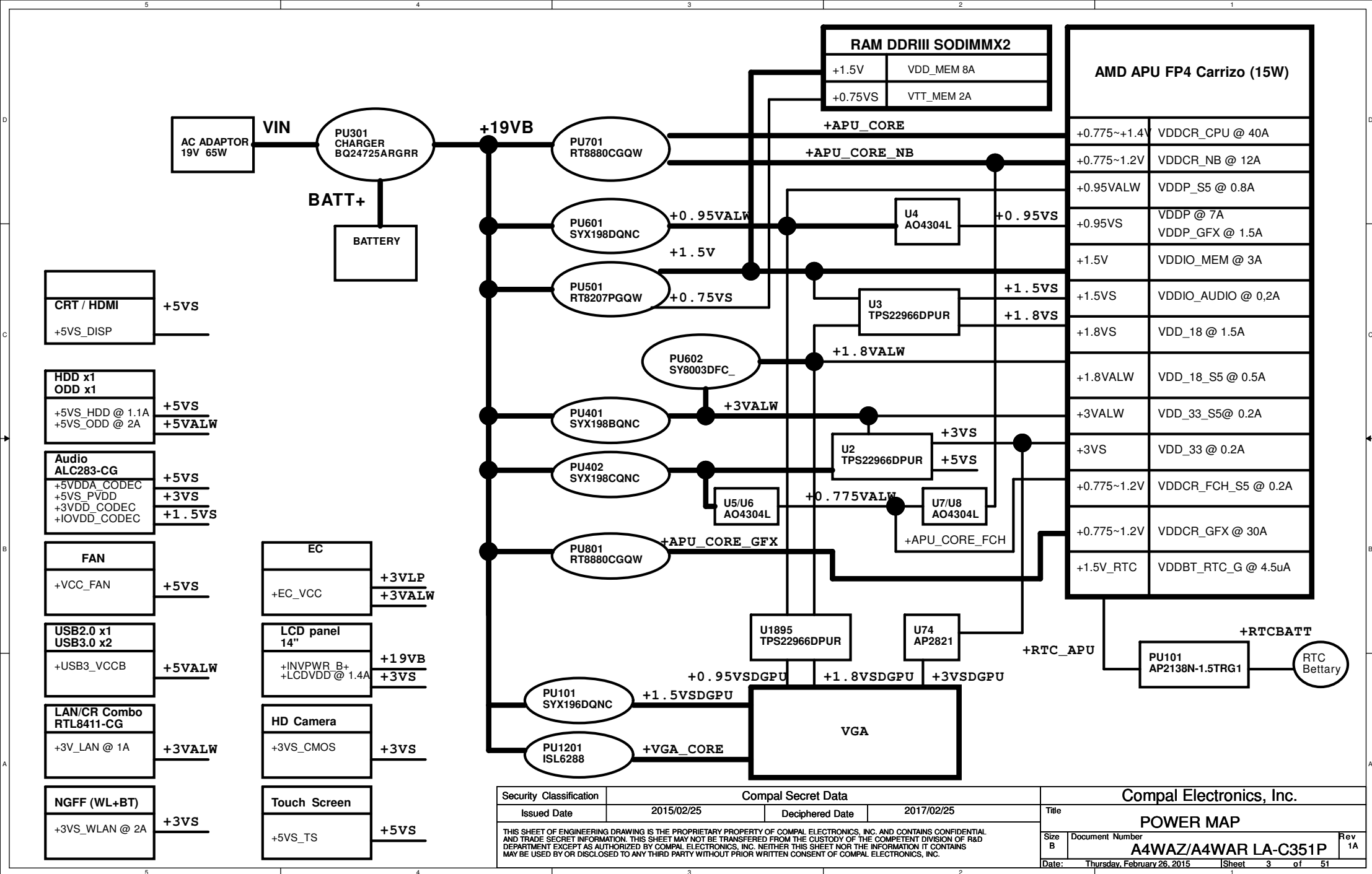
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Model Name : Sanji_CZ / Sanji_CZL



www.schematic-x.blogspot.com

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Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
+19VB	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+APU_CORE_GFX	Voltage for GFX	ON	OFF	OFF
+APU_CORE_FCH	Fusion Controller Hub Power Supply	ON	ON	ON
+0.95VALW	0.95V always on power rail	ON	ON	ON
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for APU and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+0.775VALW	0.775V always on power rail	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON
+3VSDGPU	VGA power	ON	OFF	OFF
+1.8VSDGPU	VGA power	ON	OFF	OFF
+1.5VSDGPU	VGA power	ON	OFF	OFF
+0.95VSDGPU	VGA power	ON	OFF	OFF
+VGA_CORE	VGA power	ON	OFF	OFF

EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H
			VGA Temp.		41H

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

BOM Structure	BTO Item
@	Unpop
@EMC@	EMI/ESD Unpop
EMC@	EMI/ESD pop
CZEMC@	Carrizo EMI/ESD pop
CZLEMC@	Carrizo-L EMI/ESD pop
255@	ALC255 Pop
283@	ALC283 Pop
9012@	KBC9012 Pop
9022@	KBC9022 Pop
CZ@	Carrizo Pop
CZL@	Carrizo-L Pop
EXO@	Exo Pop
MESO@	Meso Pop
CZUMA@	CZ UMA Pop
CZLUMA@	CZL UMA Pop
VGA@	DIS Pop
UMA@	UMA Pop
TPUSB@	USB to I2C Bridge Pop
ECI2C@	EC I2C Bridge Pop
TPM@	TPM Pop
BL@	Keyboard Backlight Pop
45@	HDMI Royalty
CONN@	ME Connector
JP@	Jump
RS@	R-Short
TP@	Test Point

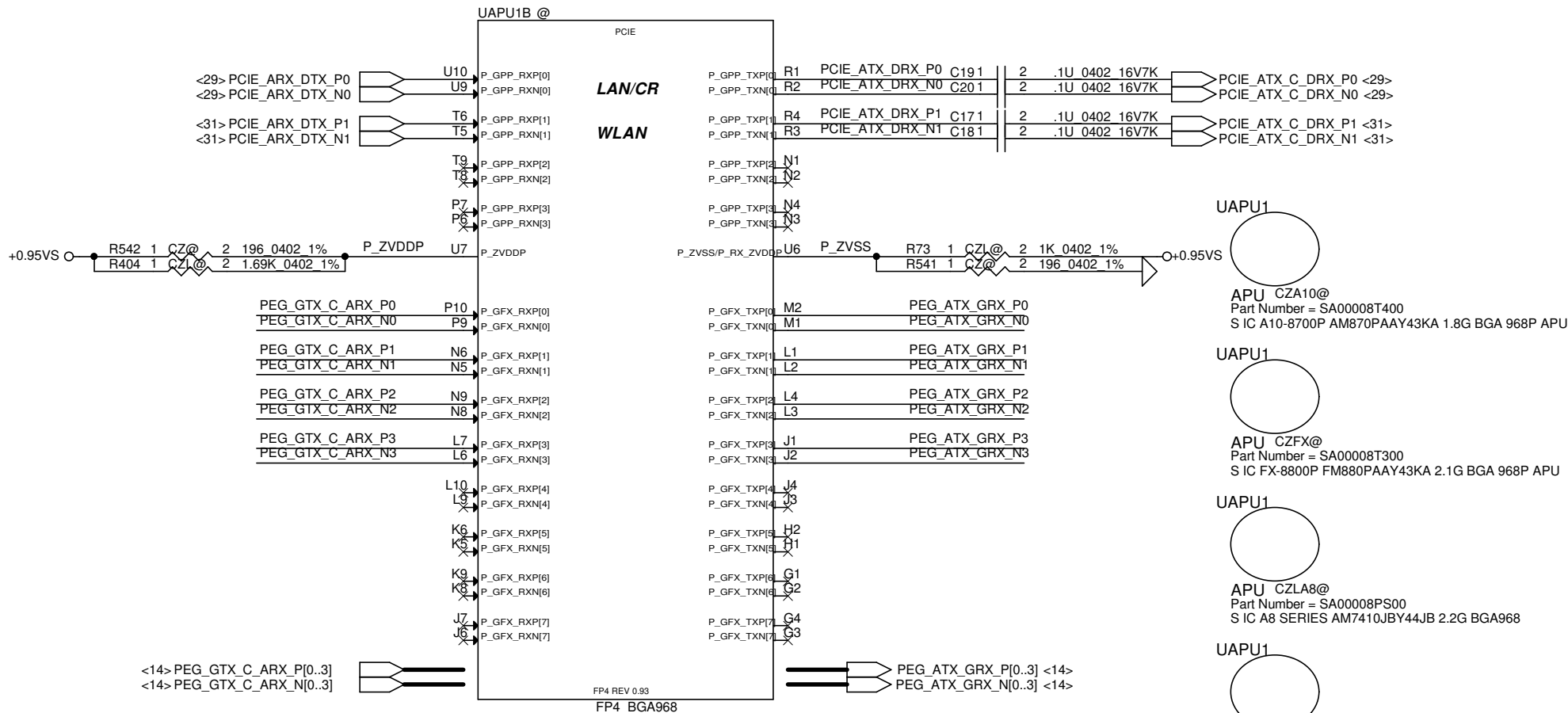
Group	Signal	Initial State	Transition	Final State
G-A	+RTC	Low	High	High
	EC_ON	Low	High	High
	+5VALW	Low	High	High
	3V_EN	Low	High	High
G-B	+3VALW	Low	High	High
	0.95_1.8VALW_PWREN	Low	High	High
	+1.8VALW/+0.95VALW	Low	High	High
	0.95V_SPOK	Low	High	High
G-C	+0.775VALW	Low	High	High
	SYSON	Low	High	High
G-D	+1.5V	Low	High	High
	SUSP#	High	Low	Low
	+5VS/+3VS/+1.8VS	Low	High	High
	+1.5VS/0.75VS	Low	High	High
	0.95VS_PWR_EN#	High	Low	Low
G-E	+0.95VS	Low	High	High
	VR_ON	Low	High	High
	+APU_CORE	Low	High	High
	+APU_CORE_NB	Low	High	High
	+APU_GFX	Low	High	High

Timing diagram showing the relationship between various signals:

- FE_GPIO1**: Signal line.
- VGA_ON**: Active-low signal line.
- +3VSDGPU**: Power supply line.
- +1.8VSDGPU/0.95VSDGPU**: Power supply line.
- VGA_ON_B**: Active-low signal line.
- +VGA_CORE**: Power supply line.
- VGA_PWRGD**: Signal line.
- +1.5VSDGPU**: Power supply line.

Board ID	PCB Revision
0	CZ EVT
1	CZL EVT
2	CZ DVT
3	CZL DVT
4	CZ PVT
5	CZL PVT
6	CZ Pre-MP
7	CZL Pre-MP

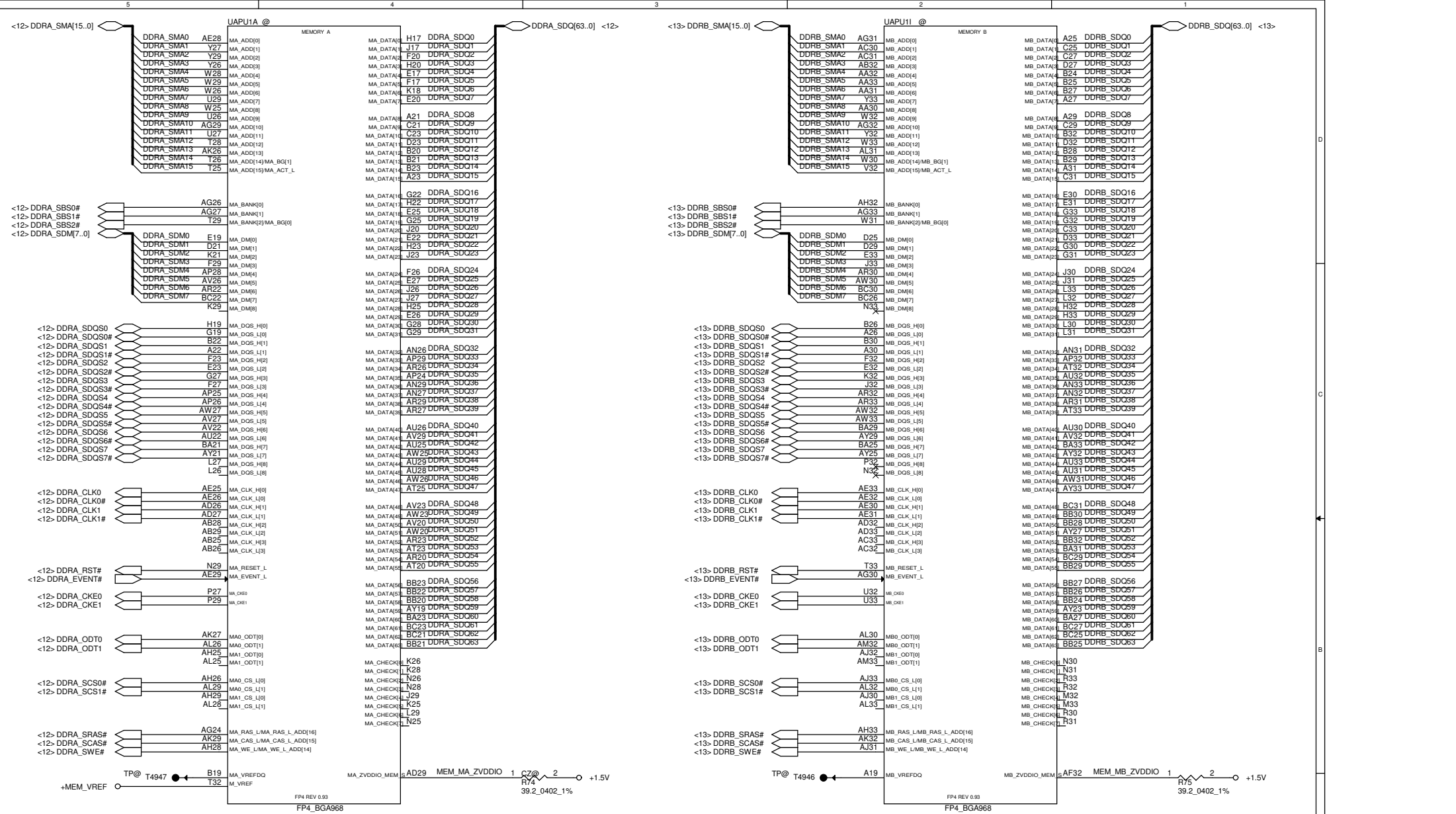
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Carrizo:
 PCIe GPP: Four x1 Gen3
 PCIe Discrete Graphics Port: PCI Gen3 x8

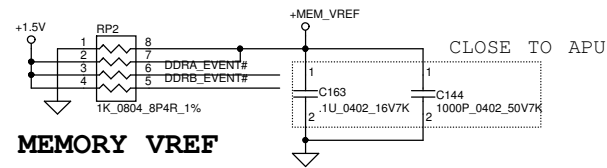
Carrizo-L:
 PCIe GPP: Four x1 Gen2
 PCIe Discrete Graphics Port: PCI Gen2 x4

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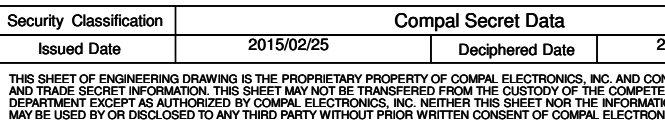
Carrizo:
DDR3 - Dual Channel
Up to 2133
Up to 2 DIMMs/Channel
uDIMM and SO-DIMM/DRAM down
1.35V and 1.5V

Carrizo-L(CHANNEL B ONLY):
DDR3 - Single Channel
Up to 1866
Up to 2 DIMMs/Channel
uDIMM and SO-DIMM/DRAM down
1.35V and 1.5V



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						Size		Document Number		Rev	
						Custom		A4WAZ/A4WAR LA-C351P		1A	
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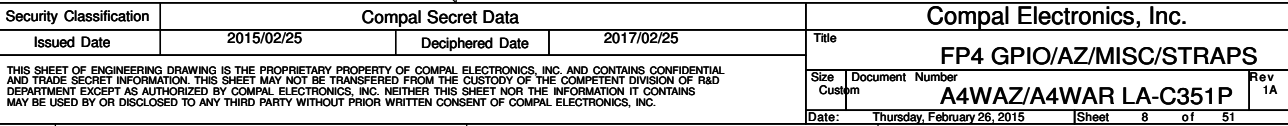
Place resistor(0ohm) for SVT on VRM side

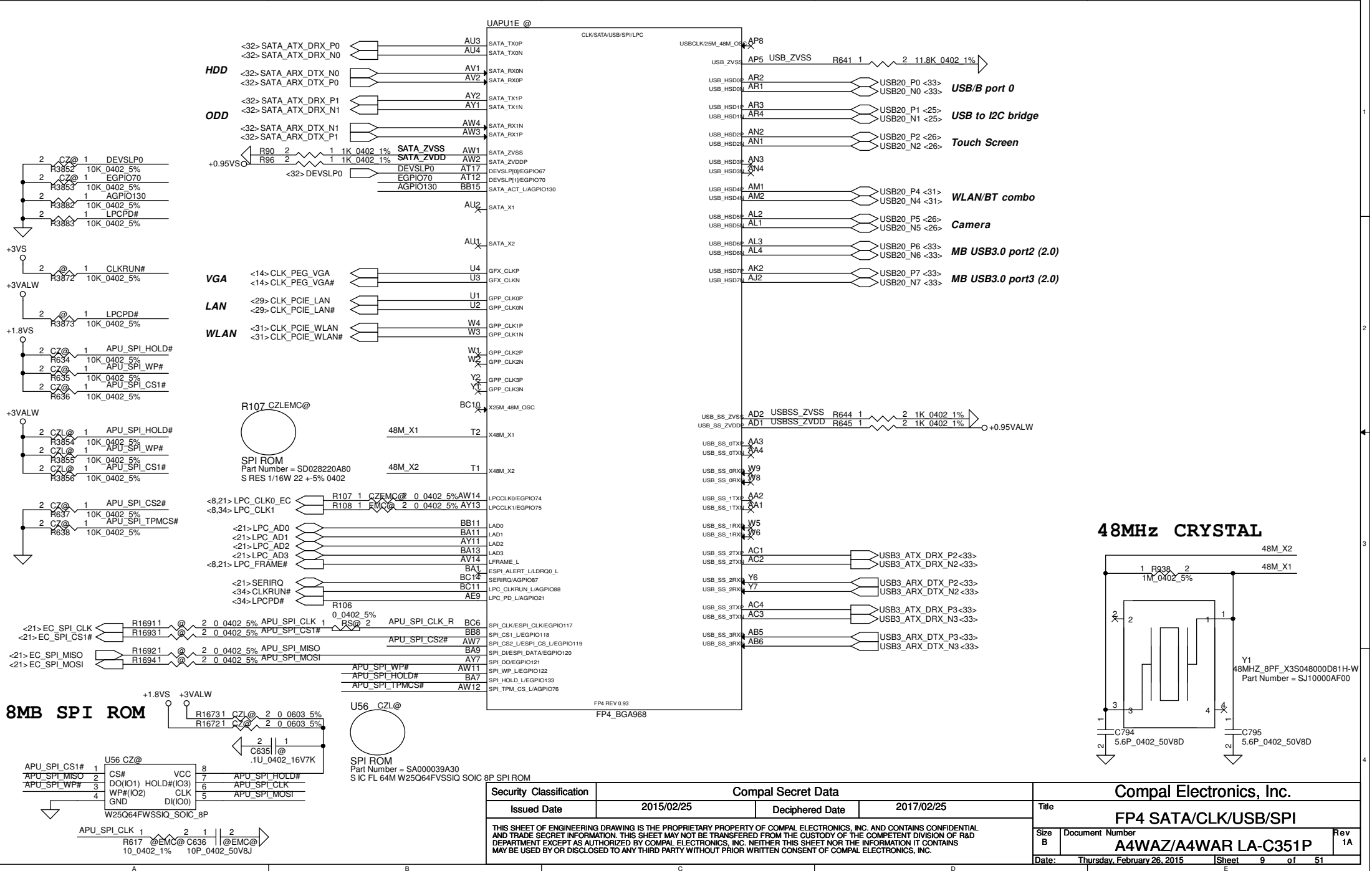


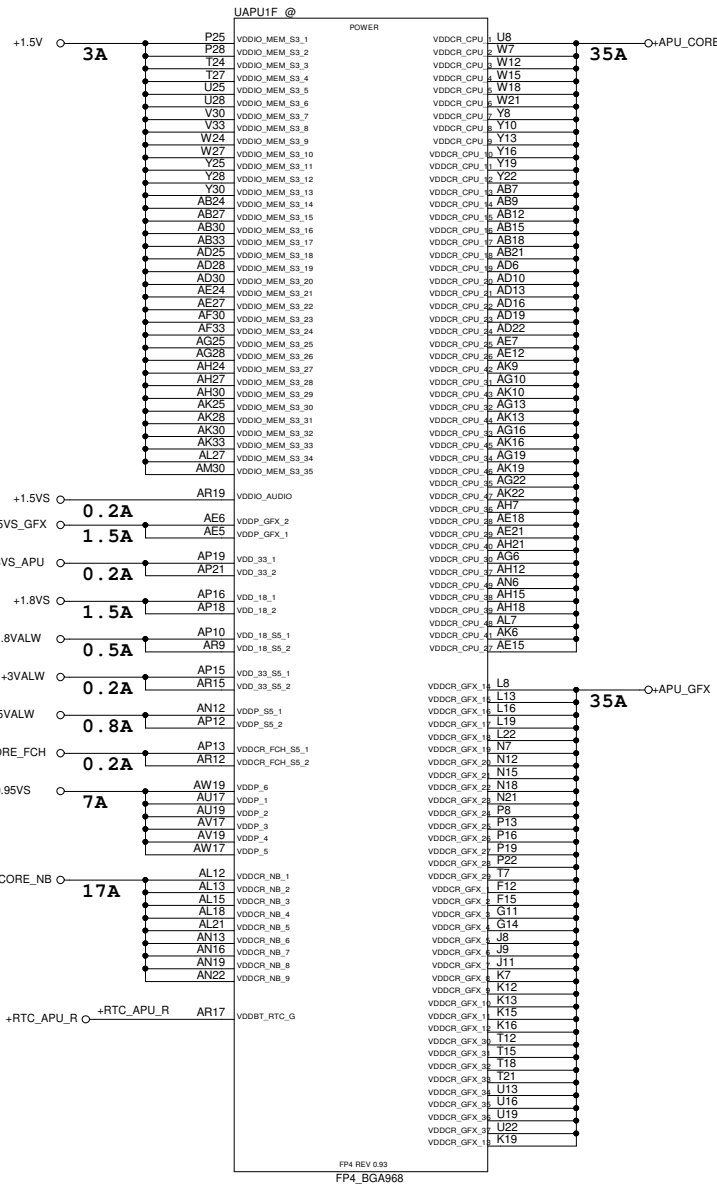
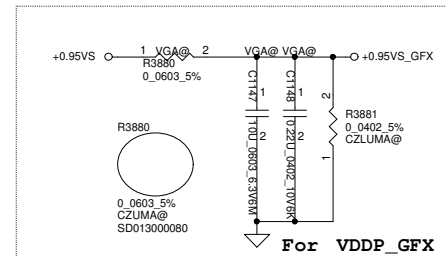
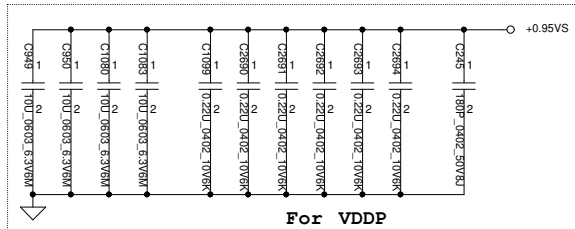
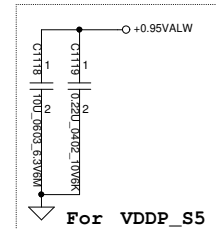
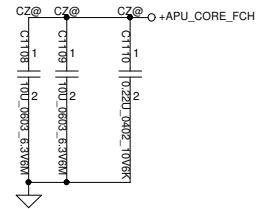
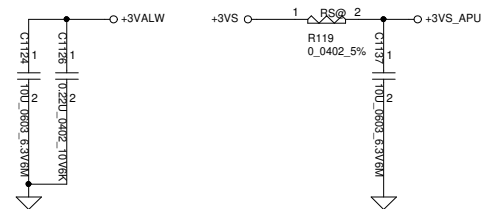
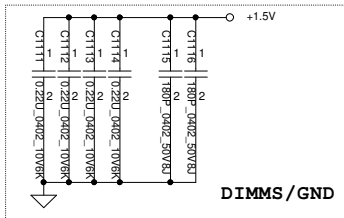
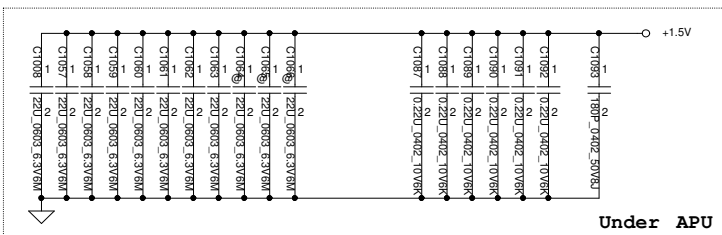
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or DP_STEREO_SYNC/TEST36 (HDMI Enable)
arrizo: Pulled up to VDD_18
arrizo-L: Pulled up to VDD_33

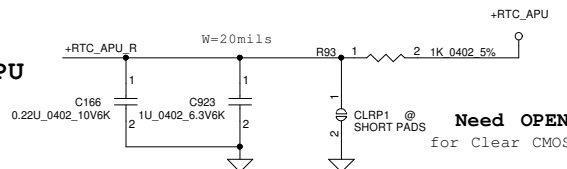
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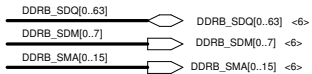
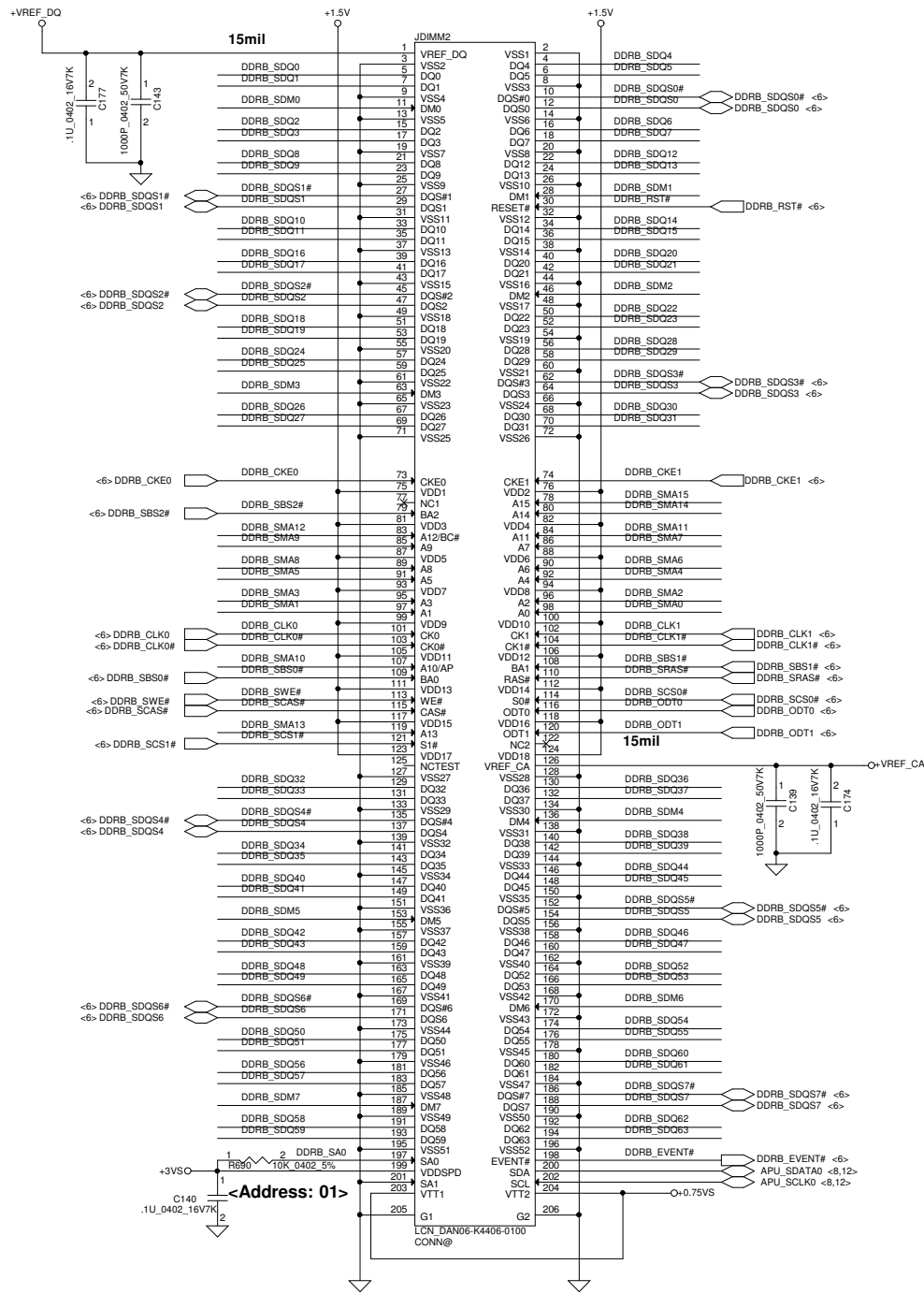




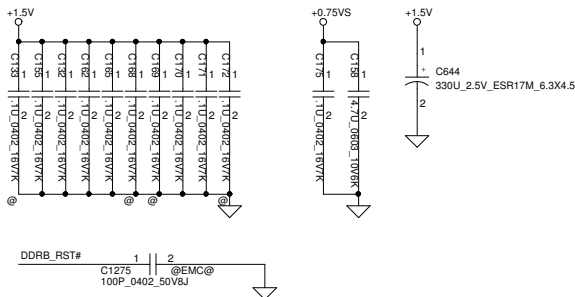
RTC OF APU



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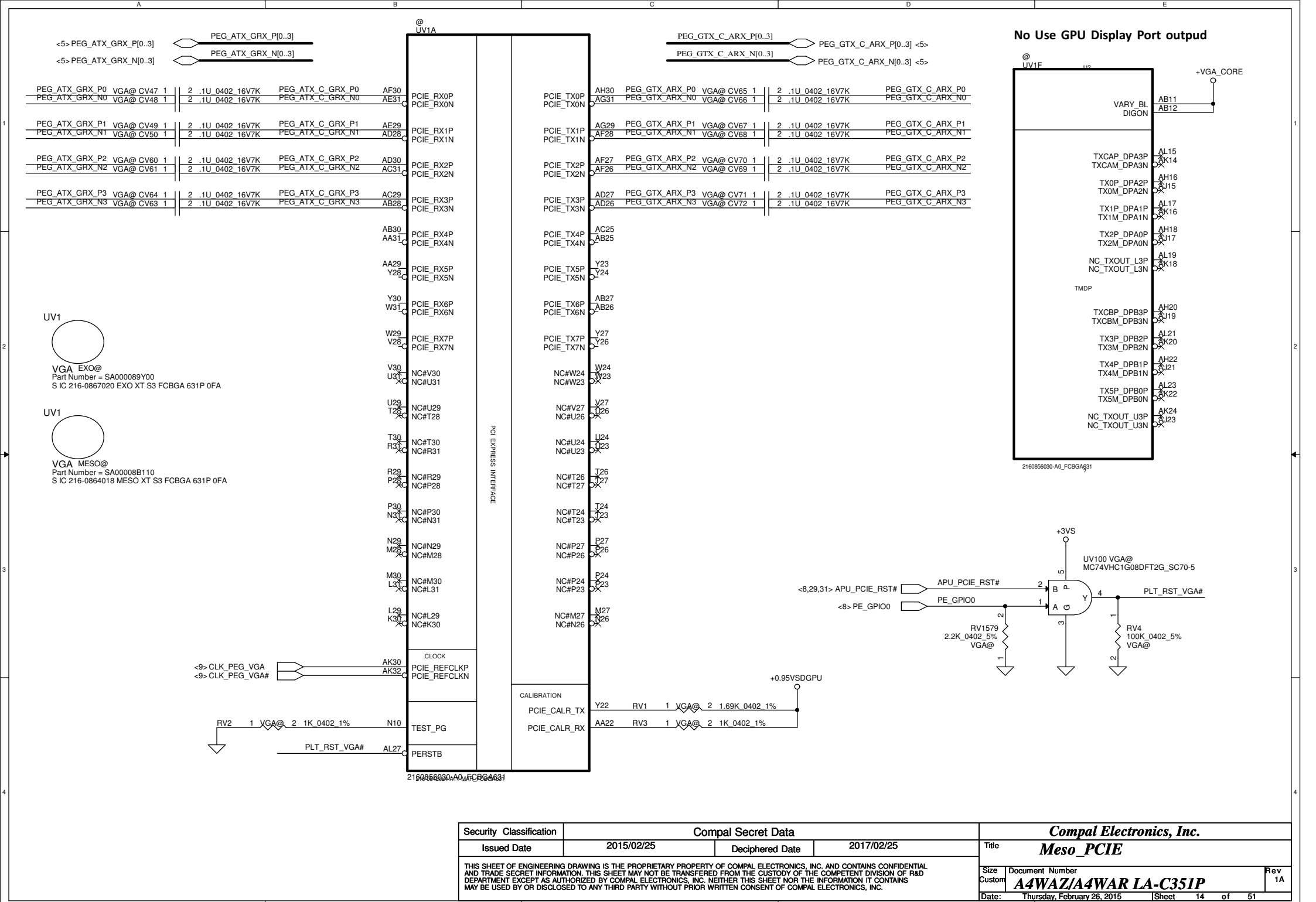


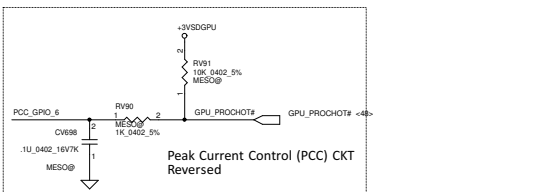
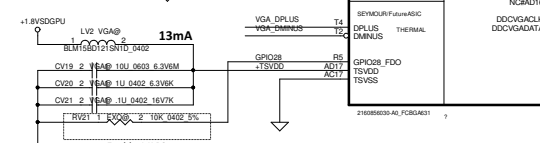
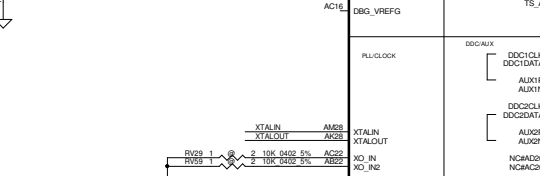
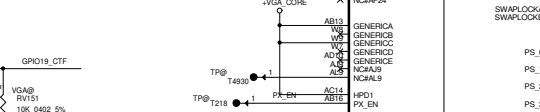
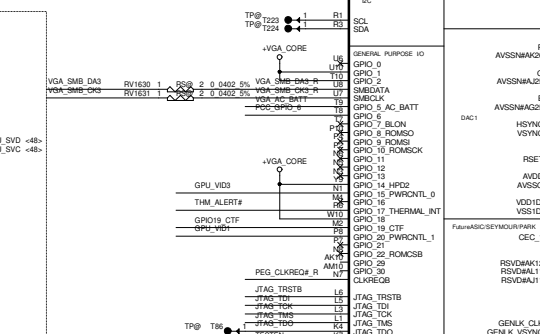
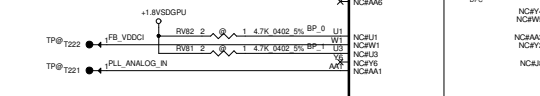
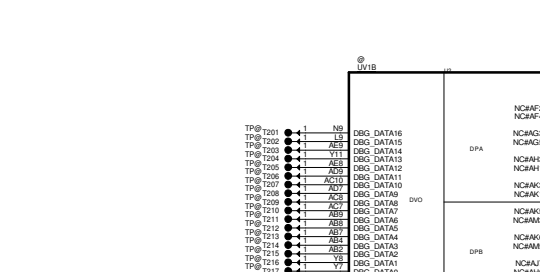
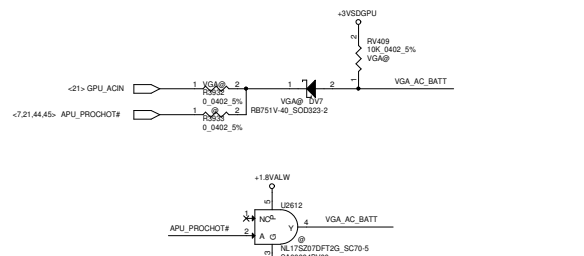
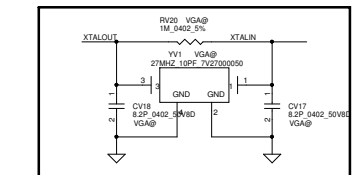
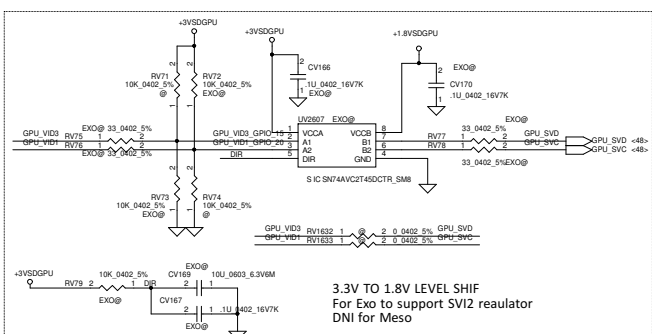
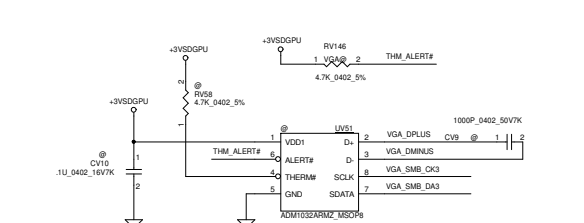
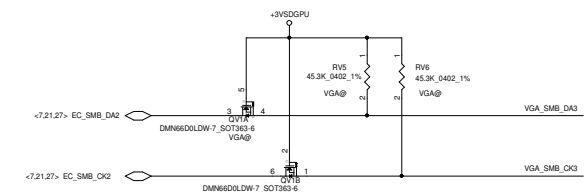
+1.5V/+0.75VS OF DIMM2



DIMM_B H:4mm STD

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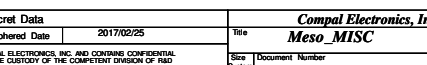
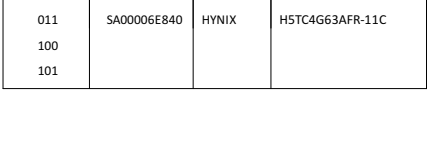
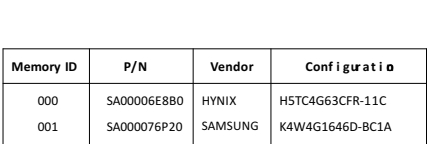
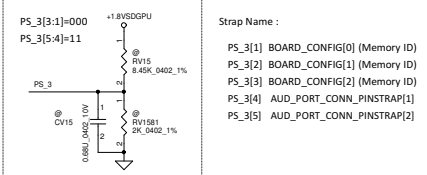
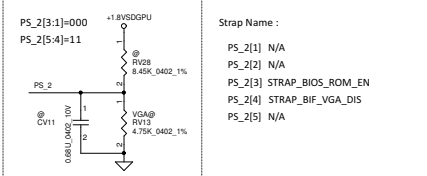
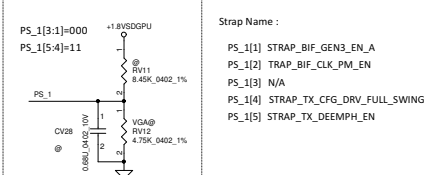
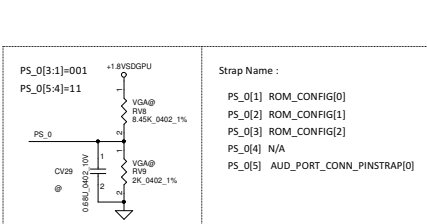
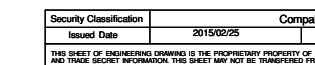
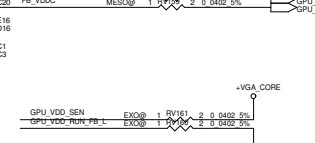
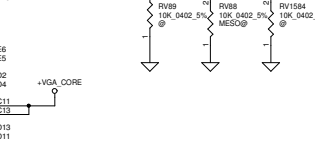
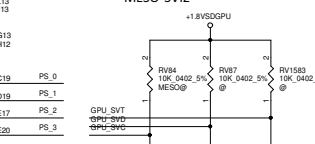
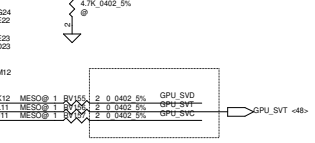
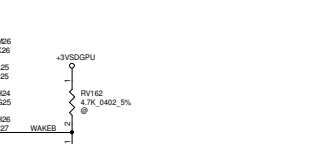




Resistor Divider Lookup Table		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are required

Capacitor Divider Lookup Table	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



Memory ID	P/N	Vendor	Configuration	Size
000	SA00006E8B0	HYNIX	H5TC4G63CFR-11C	*4 2GB
001	SA000076P20	SAMSUNG	K4W4G1646D-BC1A	*4 2GB
010	SA00008DN10	HYNIX	H5TC4G63CFR-N0C	*4 2GB
011	SA00006E840	HYNIX	H5TC4G63AFR-11C	*4 2GB
100				
101				

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				Date: Thursday, February 26, 2015	Sheet 15 of 51

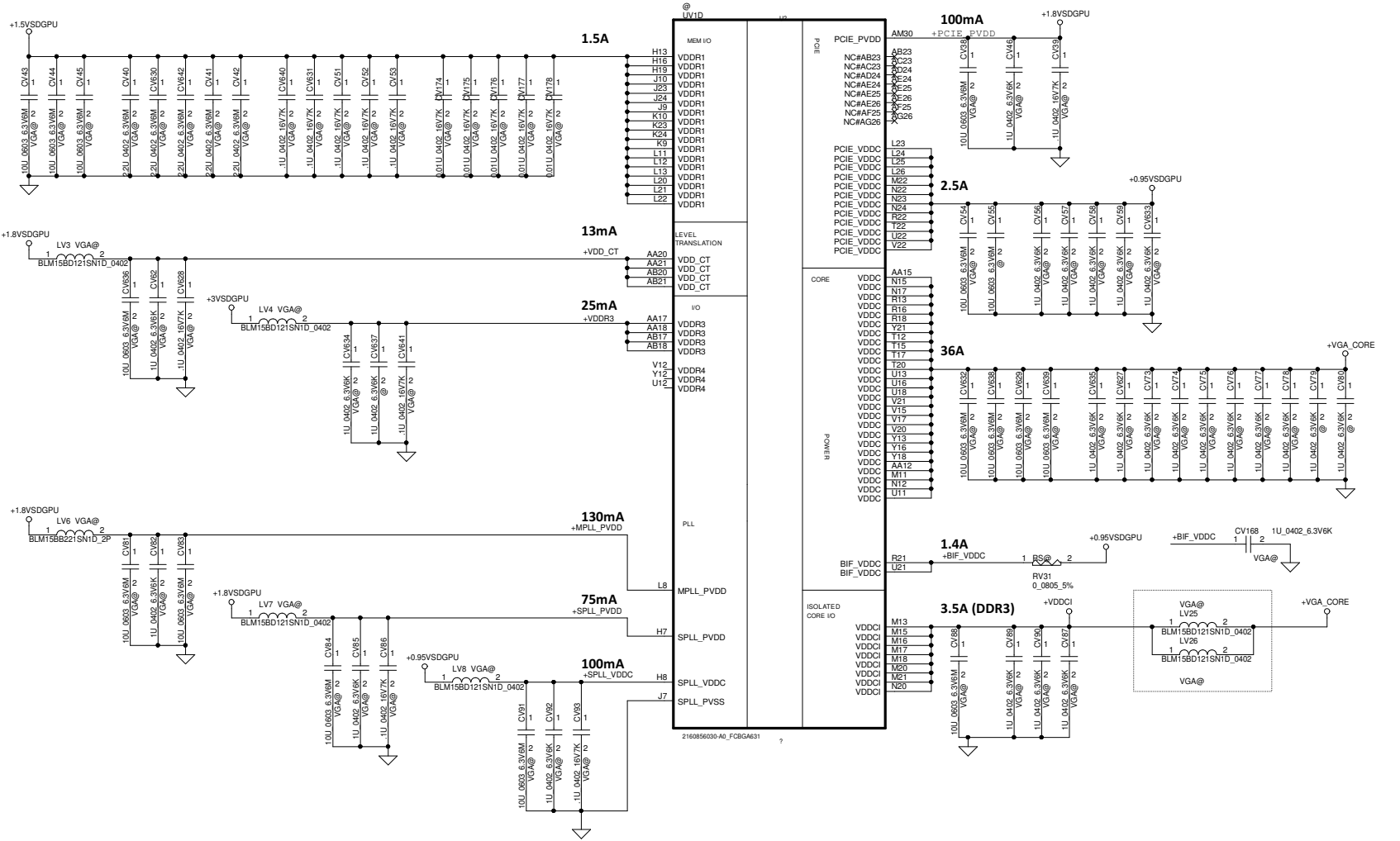
+VGA_CORE	10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)
VDDCI	3.5A	1	3
			0

+0.95VSDGPU	10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)
BIF_VDDC	1.4A	0	1
			0
SPLL_VDDC	100mA	1	1
			1

+1.5VSDGPU	10uF	2.2uF	0.1uF
			0.01uF
VDDR1 1.5A	3	5	5
			5

+1.8VSDGPU	10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1
MPLL_PVDD	130mA	1	1
SPLL_PVDD	75mA	1	1
			1
VDDR4	(300mA)	0	0
			0
VDD_CT	13mA	1	1
			1
+TSVDD	13mA	1	1
			1
+DP_VDDR	0	0	0
			0
+DP_VDDC	0	0	0
			0

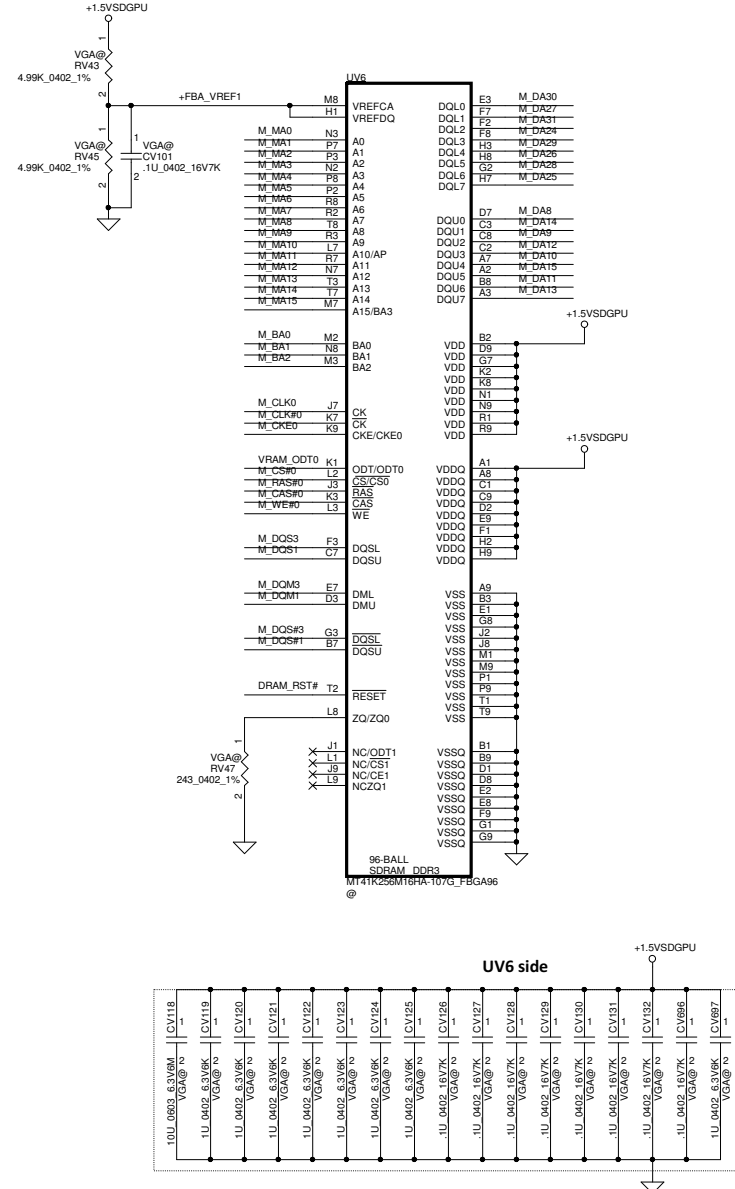
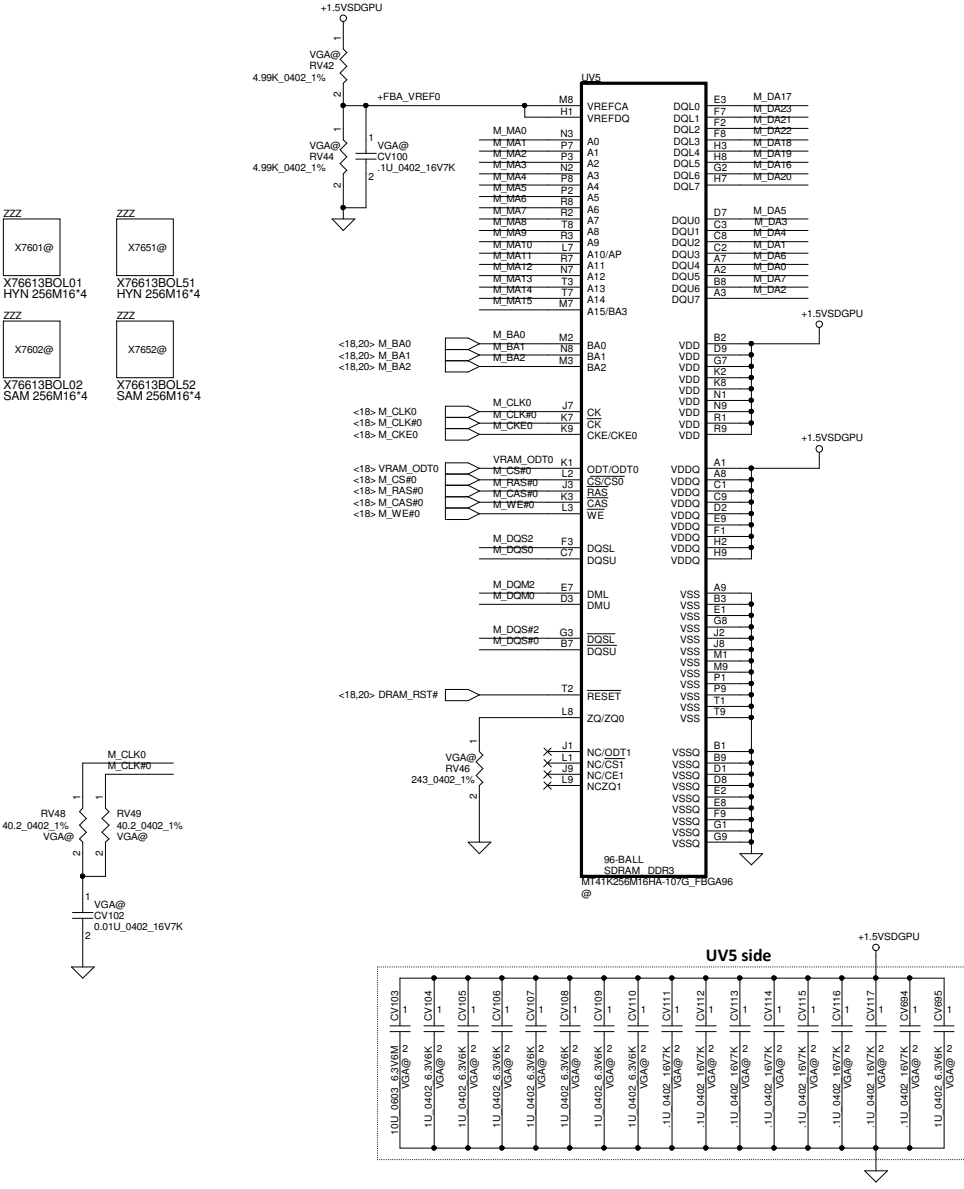
+3VGS	10uF	1uF	0.1uF
			0.1uF
VDDR3	25mA	0	2 (1@)
			1



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Size	Document	Number		Rev	
Custom	A4WAZ/A4WAR	LA-C351P		1A	
Date:	Thursday, February 26, 2015	Sheet	17	of 51	

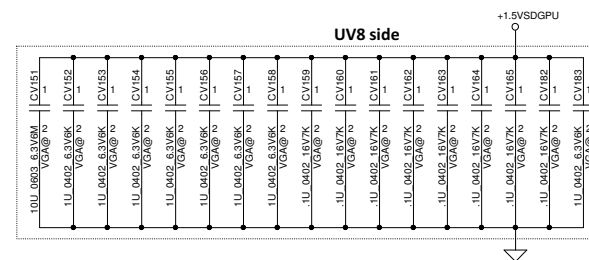
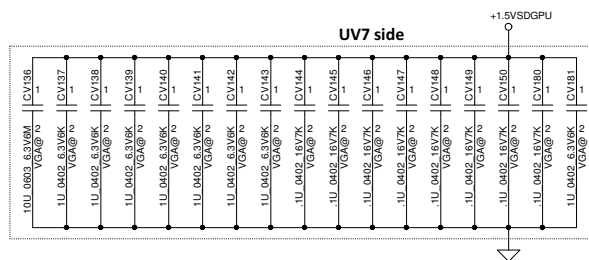
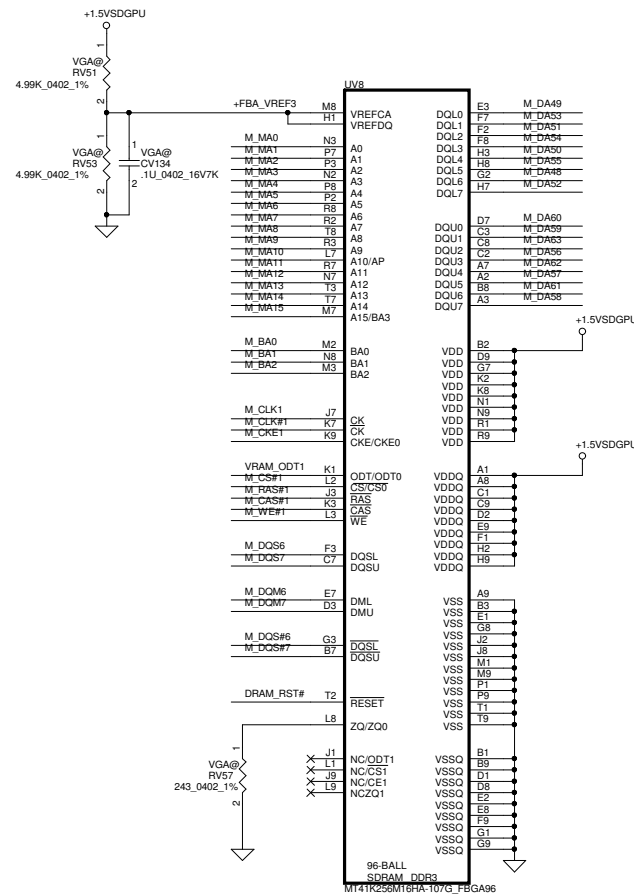
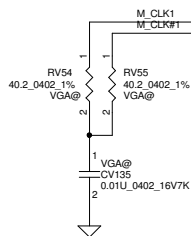
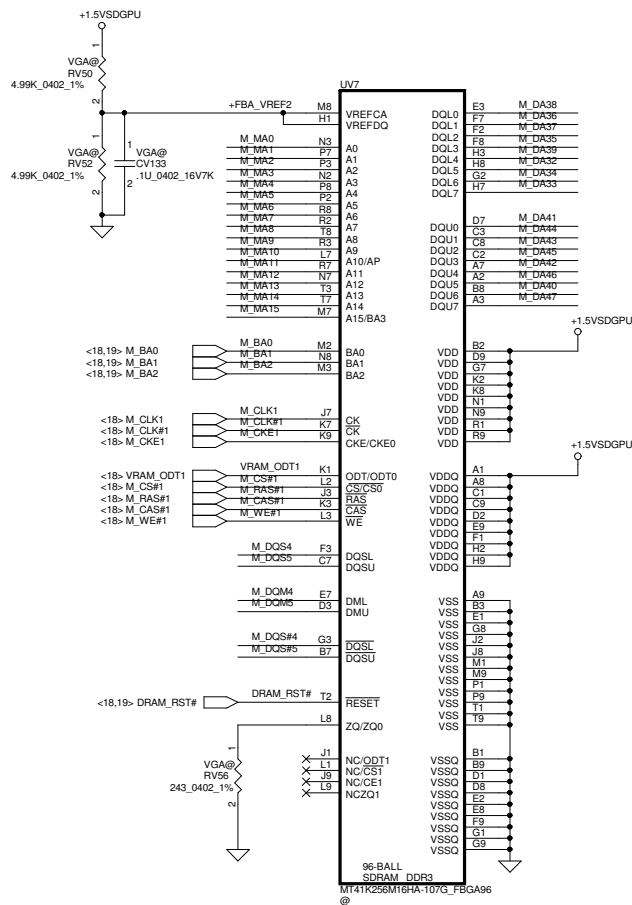
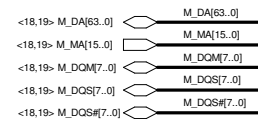
Memory Partition A - Lower 32 bits

- <18,20> M_DA[63..0]
- <18,20> M_MA[15..0]
- <18,20> M_DQM[7..0]
- <18,20> M_DQS[7..0]
- <18,20> M_DQS# [7..0]

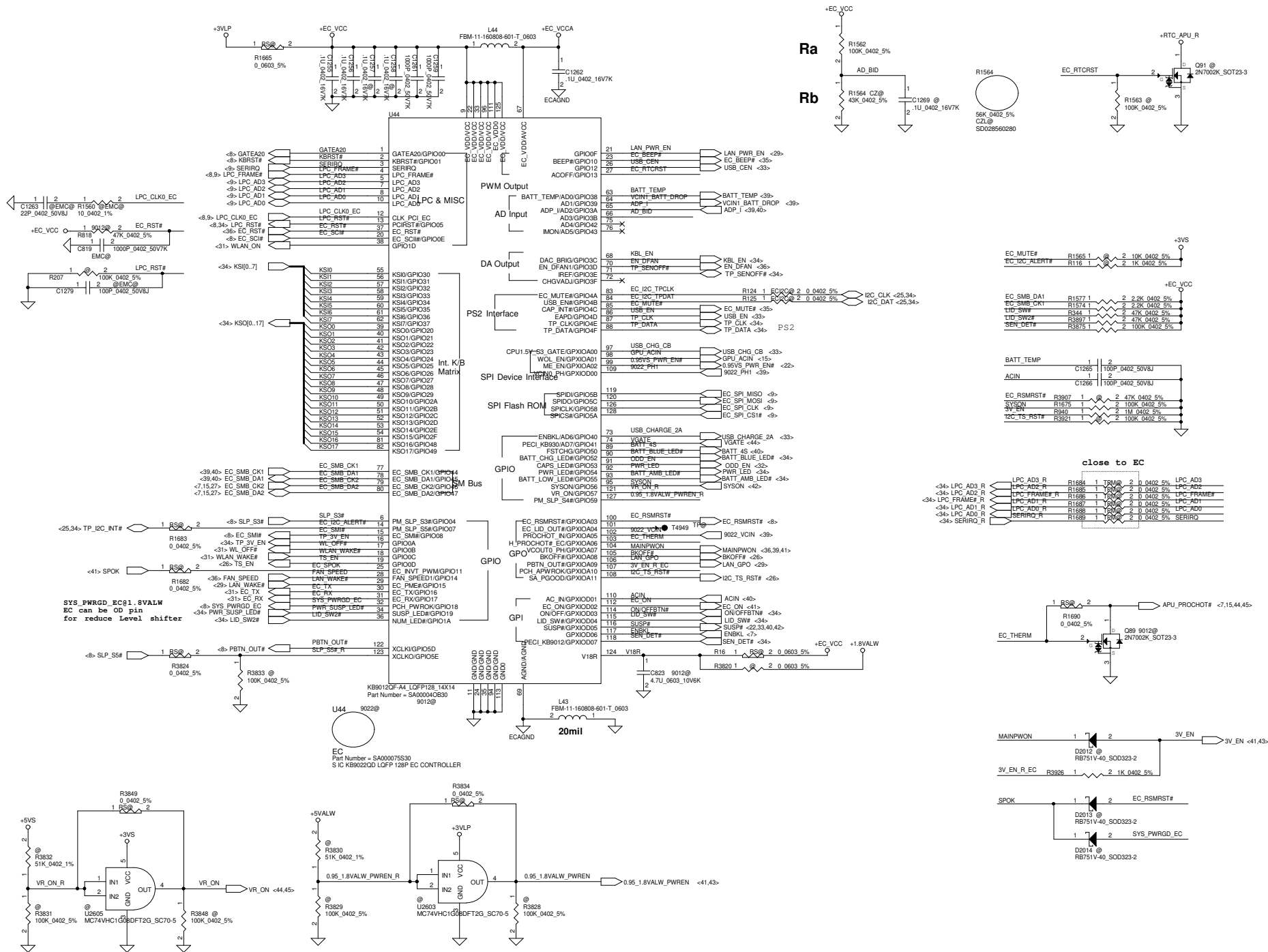


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Issued Date	2015/02/25	Deciphered Date	2017/02/25	Title	VRAM_DDR3_Lower
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				Custom	A4WAZ/A4WAR LA-C351P
				Date:	Thursday, February 26, 2015
				Sheet	19 of 51
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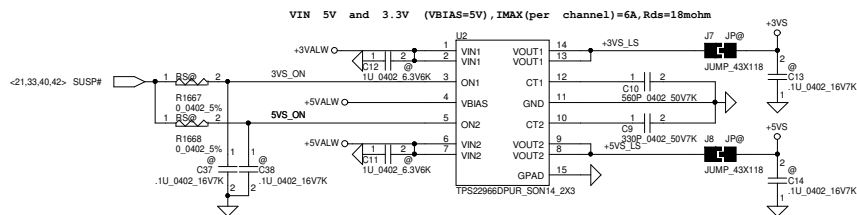
Memory Partition A - Upper 32 bits



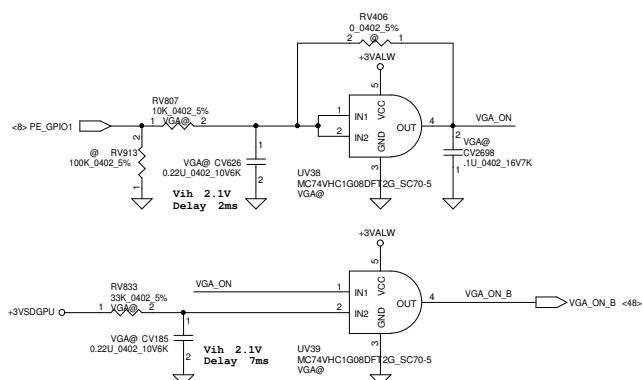
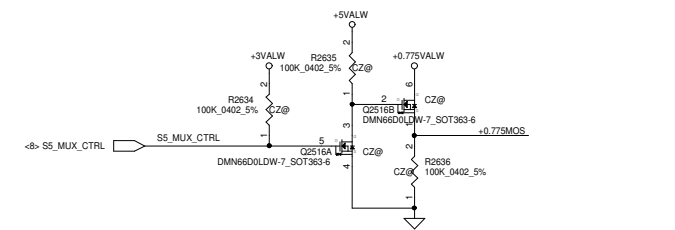
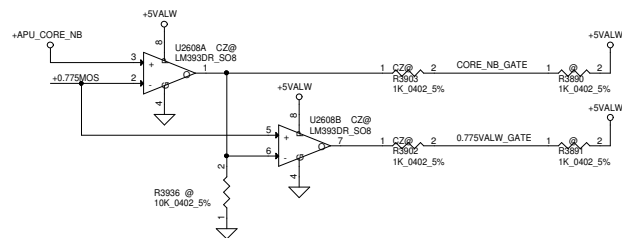
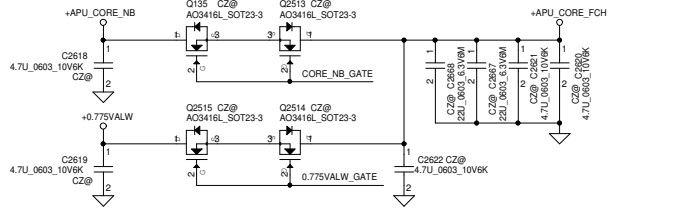
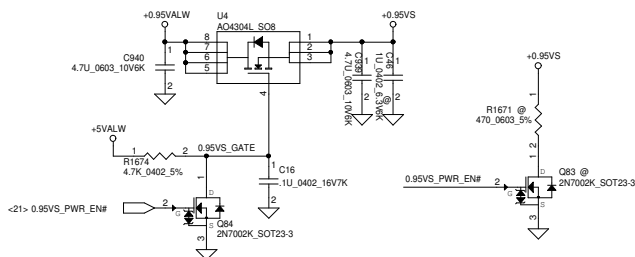
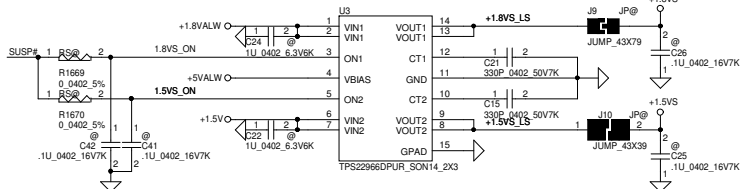
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Issued Date	2015/02/25	Deciphered Date	2017/02/25	Title	VRAM_DDR3_Upper	
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				Custom	A4WAZ/A4WAR LA-C351P	
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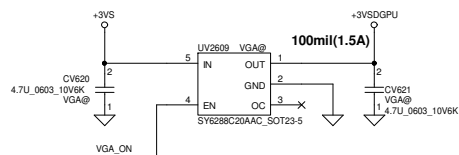
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2017/02/25		
Title		EC ENE-KB9012
Size	Document Number	A4WAZ/A4WAR LA-C351P
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VIN 1.8V and 1.5V (VBIAS=5V), IMAX(per channel)=6A, Rds=18mohm

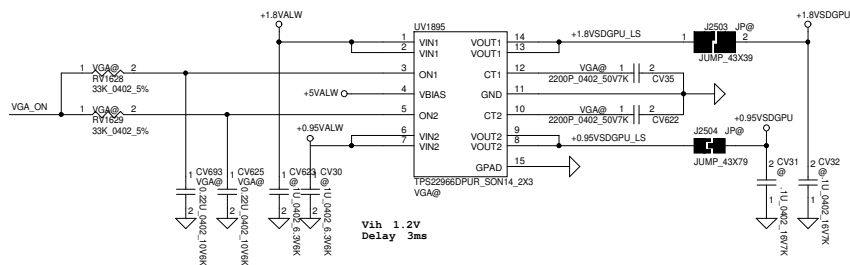


+3VSDGPU TO +3VSDGPU

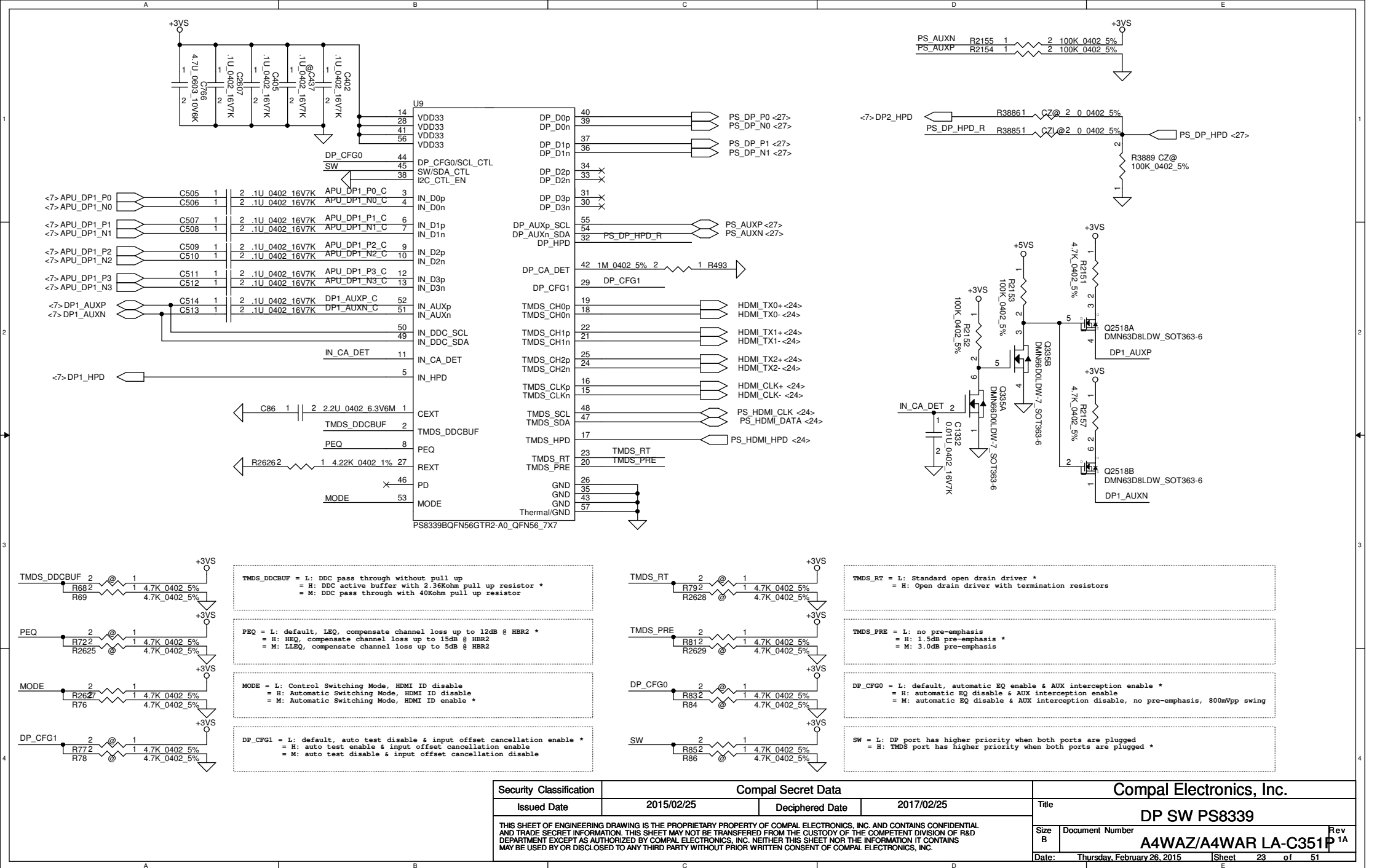


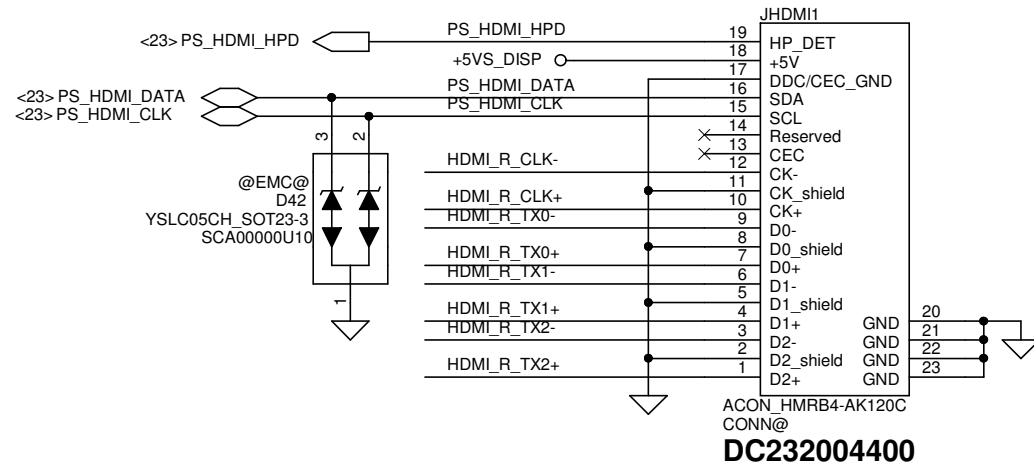
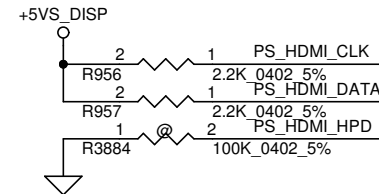
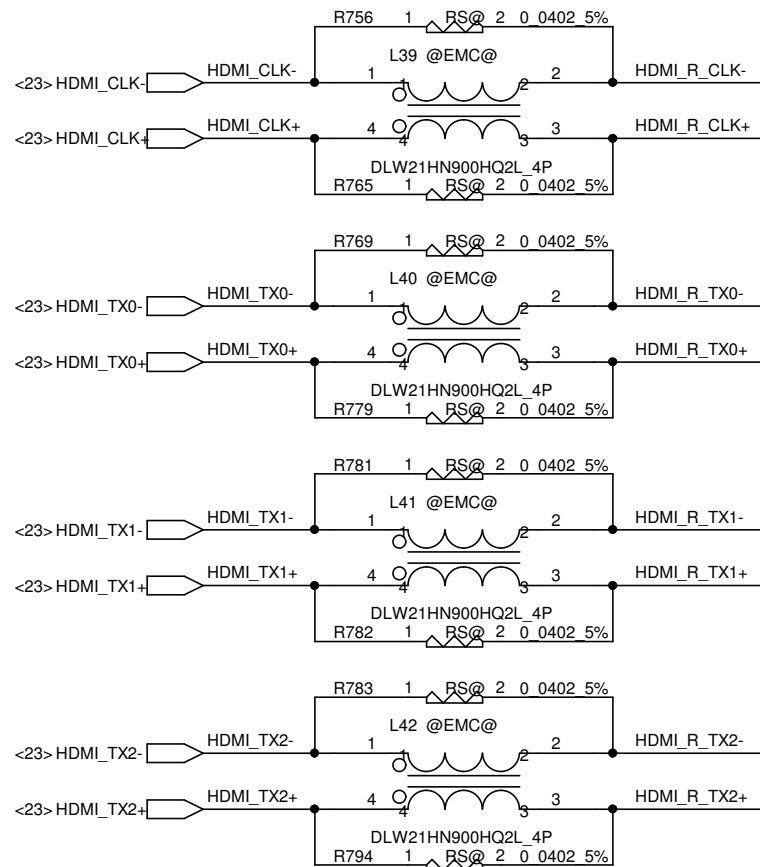
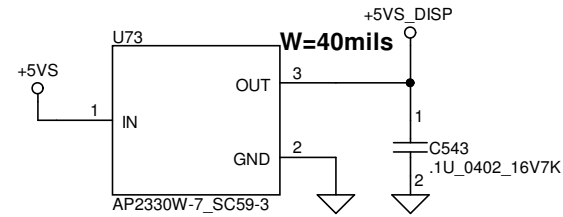
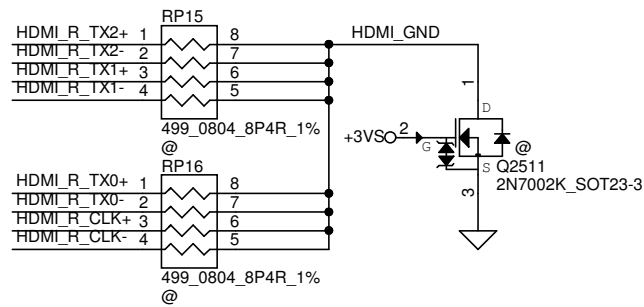
+1.8VALW TO +1.8VSDGPU
+0.95VALW TO +0.95VSDGPU
Load switch

VIN 1.8V and 0.95V (VBIAS=5V), IMAX(per channel)=6A, Rds=18mohm

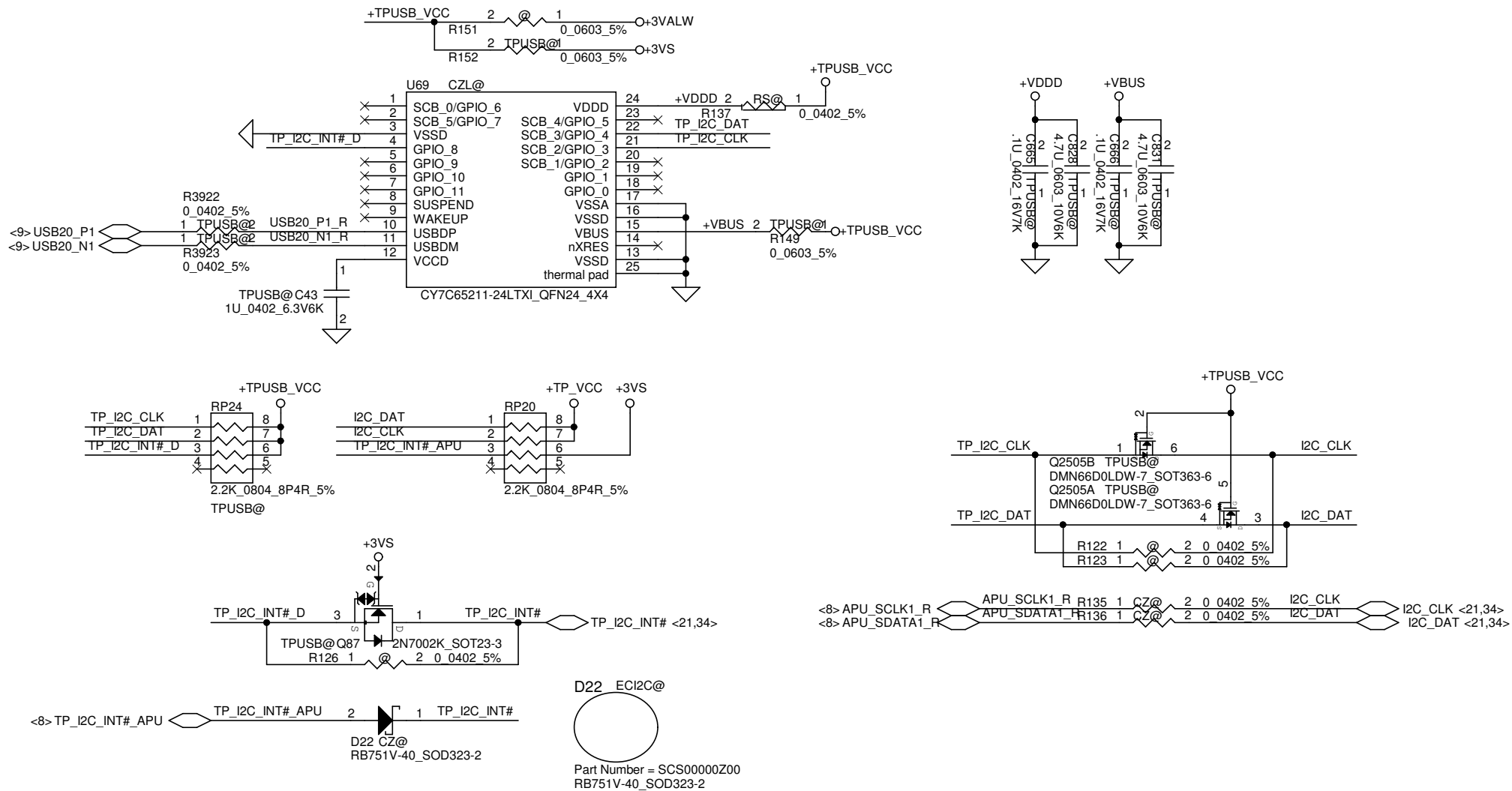


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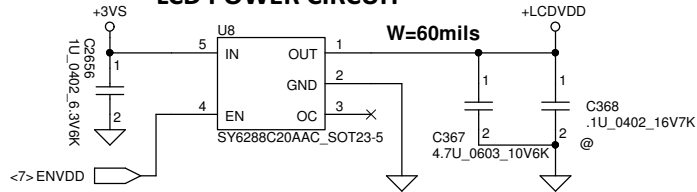


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Size	Document Number	A4WAZ/A4WAR LA-C351P			Rev 1A
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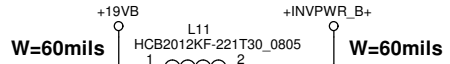
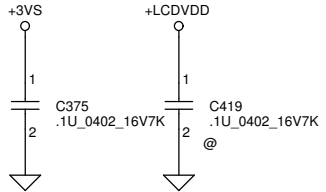


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				Size Custom	Document Number A4WAZ/A4WAR LA-C351P
				Date:	Thursday, February 26, 2015
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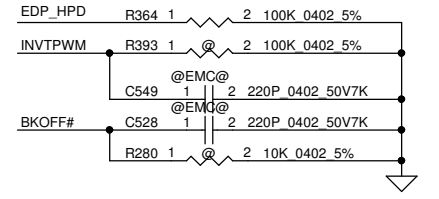
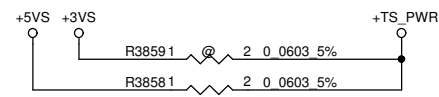
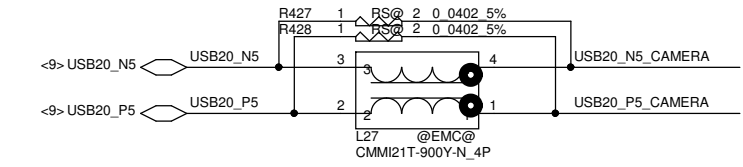
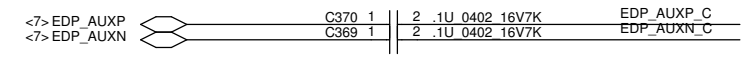
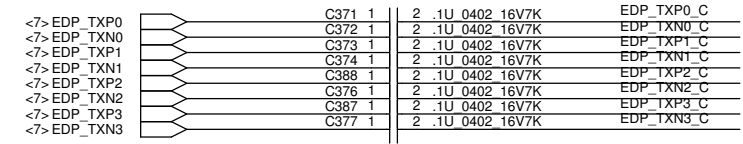
LCD POWER CIRCUIT



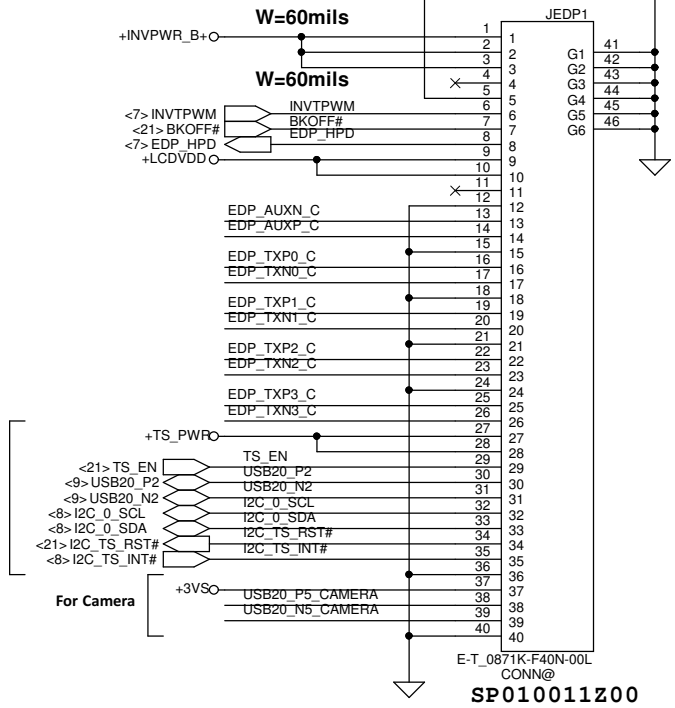
Place closed to JEDP1



SM01000EJ00 3000ma
220ohm@100mhz
DCR 0.04

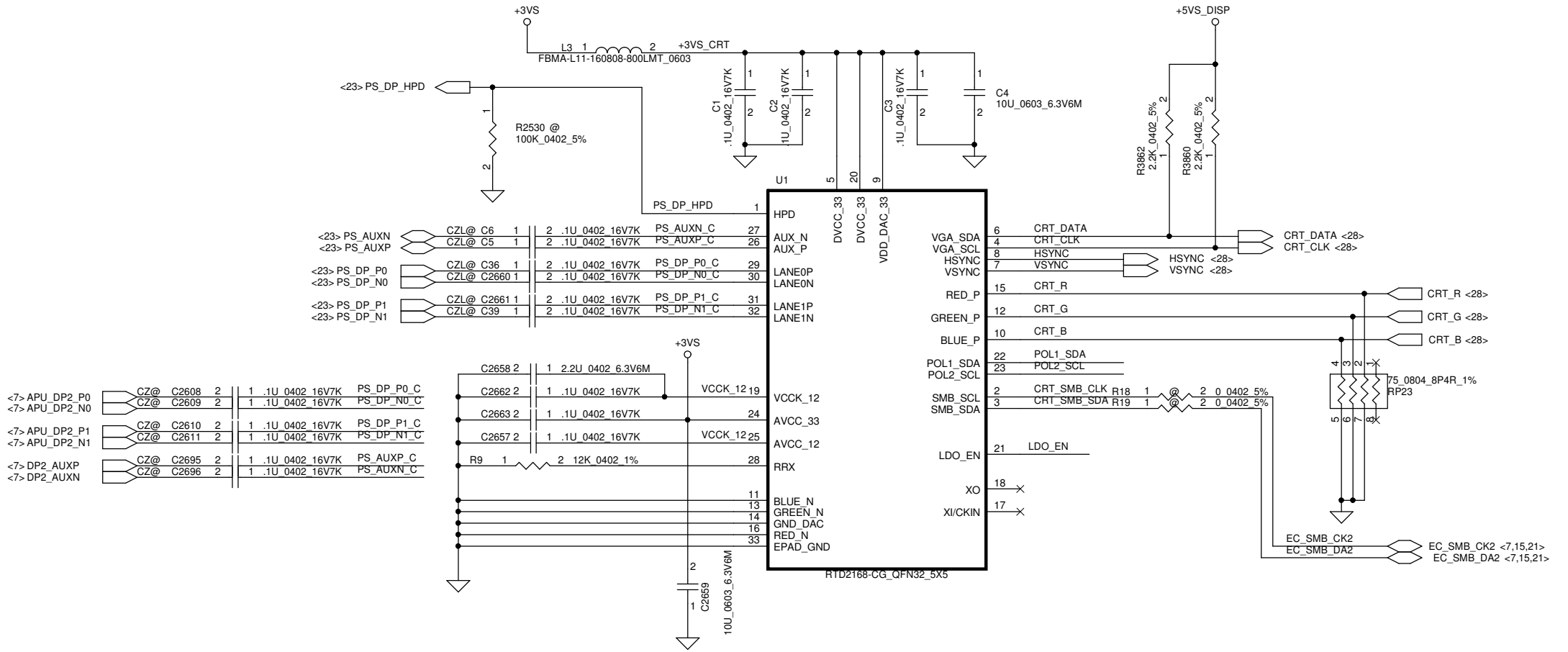


LED PANEL Conn.



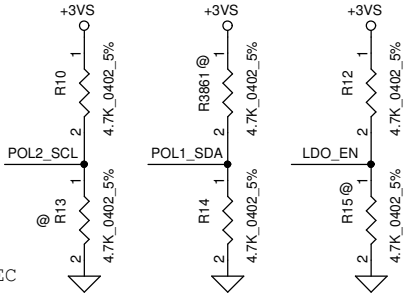
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CONN@
SP010011Z00

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Size Custom		Document Number		Rev 1A	
		A4WAZ/A4WAR LA-C351P			
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		POL_SDA	
		0	1
POL_SCL	0	X	EP
	1	*ROM	EEPROM

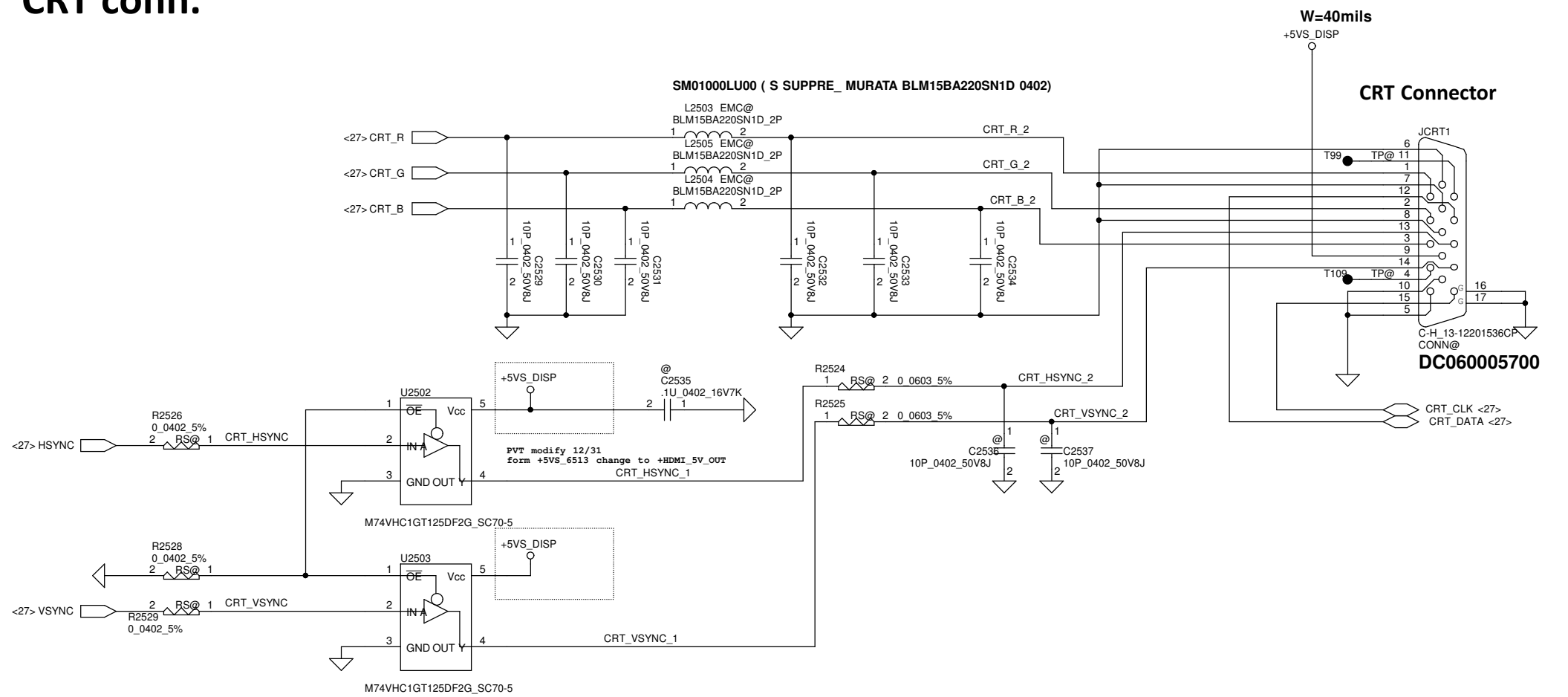
ROM: Internal ROM
EP: Programmed external EC
EEPROM: External ROM



LDO_EN:
*1: Internal 1.2V
0: External 1.2V

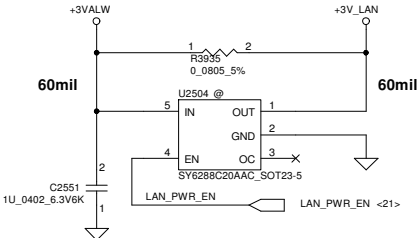
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2015/02/25		Deciphered Date		2017/02/25		Title			
								DP-VGA RTD2168			
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						Custom		A4WAZ/A4WAR LA-C351P		1A	
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CRT conn.

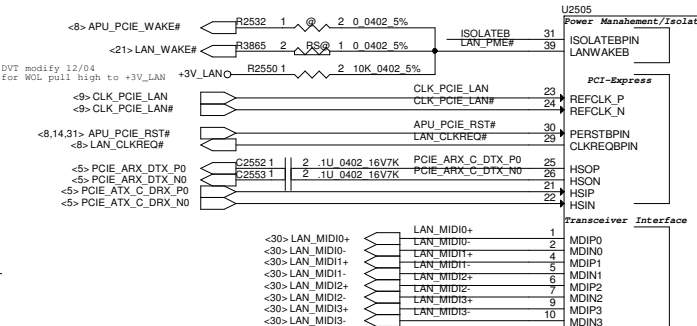
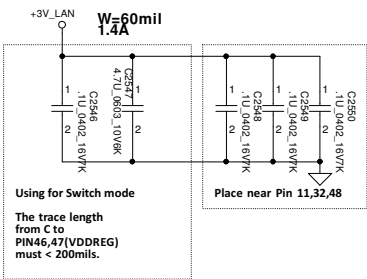
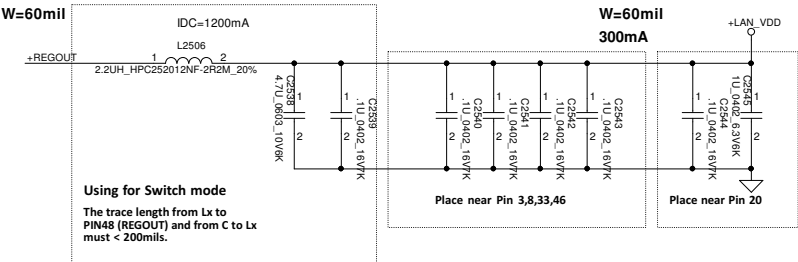


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Date: Thursday, February 26, 2015		Sheet 28 of 51		Size Custom	Rev 1A

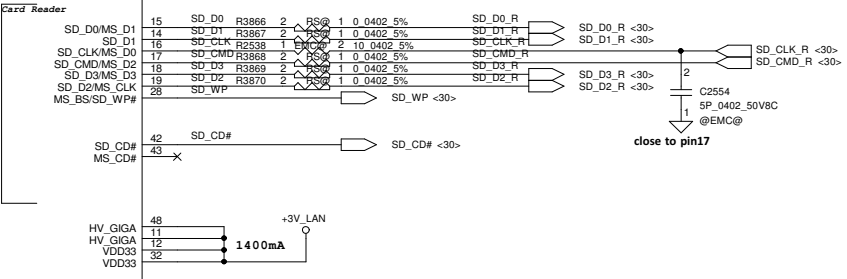
LAN-RTL8411B



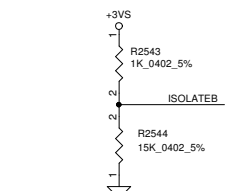
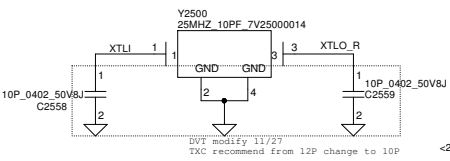
From EC
High active
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A
+3V_LAN Rising time must >0.5ms and <100ms

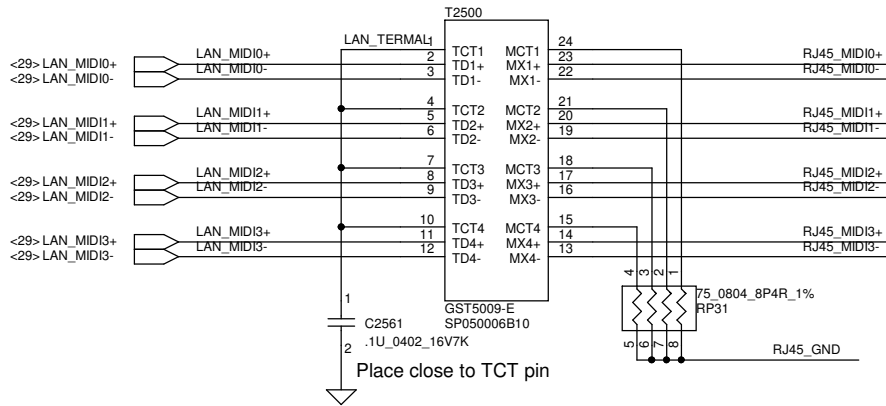


PVT modify 01/06
R2534, R2537, R2539, R2535, R2536
change to R-short

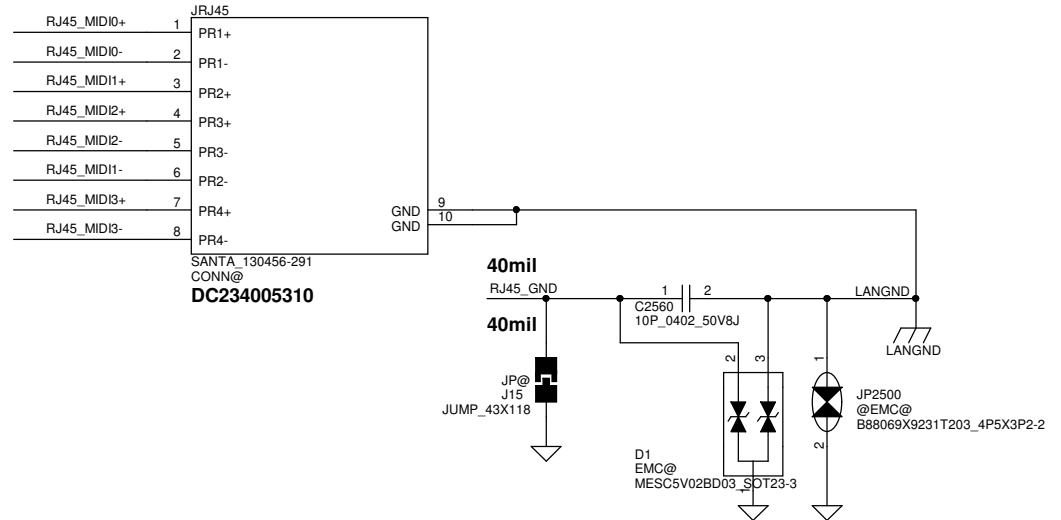


	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

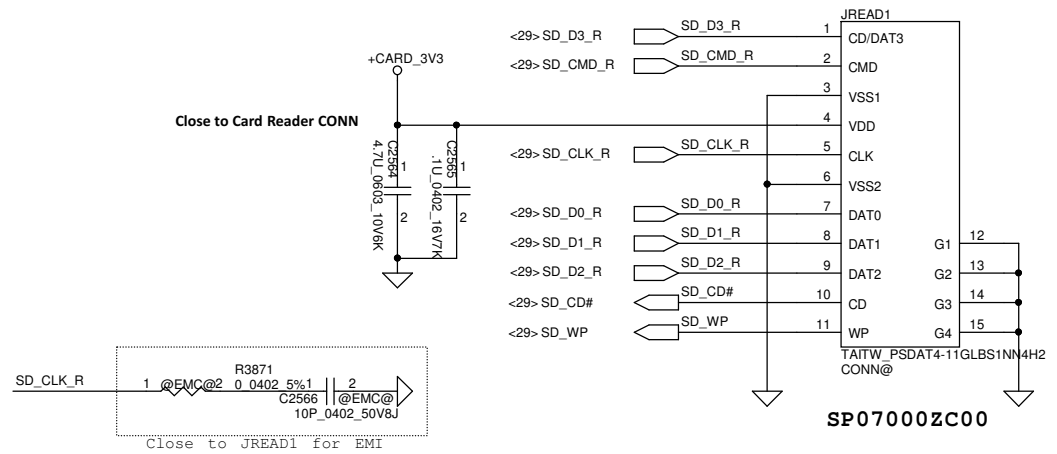




LAN Connector

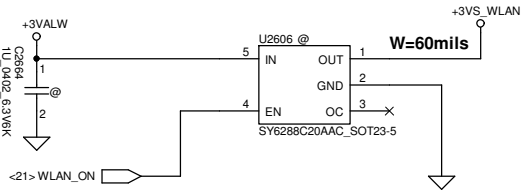
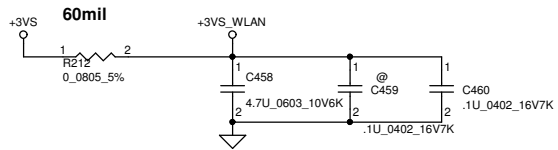


Card Reader Connector



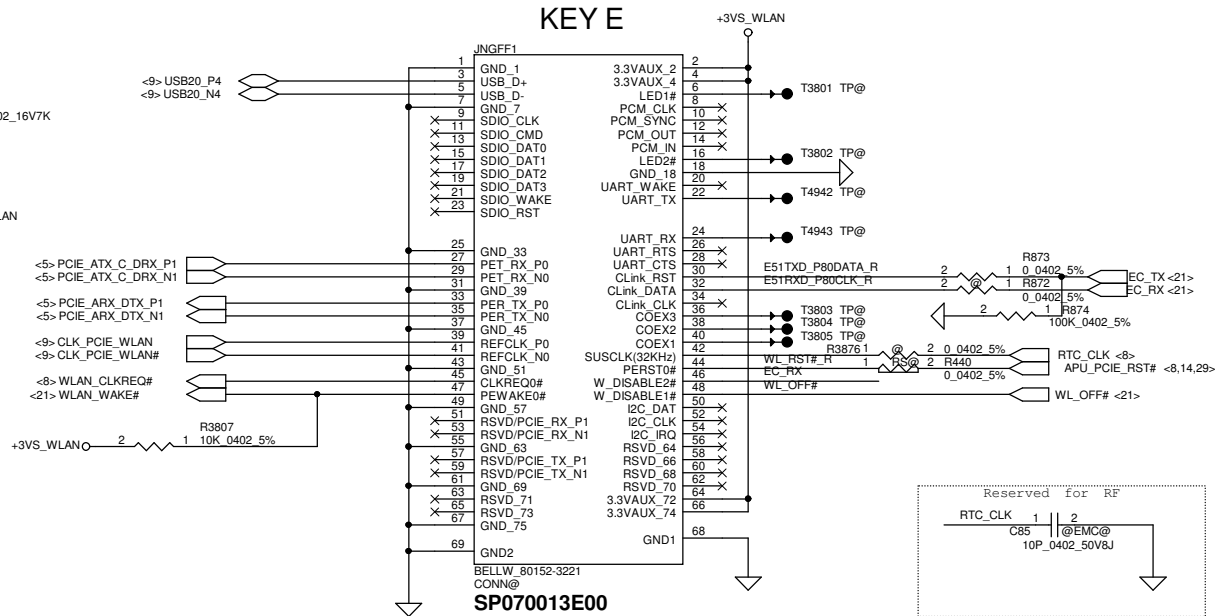
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Issued Date	2015/02/25	Deciphered Date	2017/02/25	Title	
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Size		Document Number		Rev	
Custom		A4WAZ/A4WAR LA-C351P		1A	
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Wireless LAN



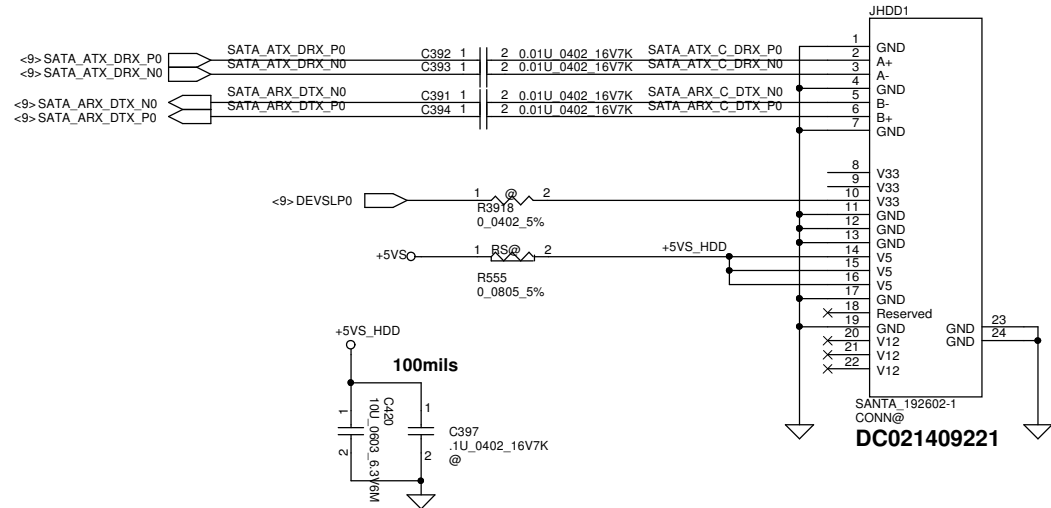
NGFF WL+BT (KEY E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLK1	73
70	UMI_Power_SPC(I/O)(3.3V)	RESERVED/REFCLK1P	71
68	UMI_Power_SNK(CMREQ2)P	GND	69
66	UMI_SWP/PEST1P	Reserved/PEPn1	67
64	RESERVED	Reserved/PEPn1	65
62	ALERT1(O)(0.3V)	GND	63
60	Q2 CLK (O)(0.3V)	Reserved/PTn1	61
58	Q2 DATA (I/O)(0.3V)	Reserved/PT1p1	59
56	W_DISABLE1(O)(0.3V)	GND	57
54	Reserved/W_DISABLE2(O)(0.3V)	PEWakeUp(O)(0.3V)	55
52	PERST0(O)(0.3V)	CLKREQ0(O)(0.3V)	53
50	SUSCLK3MHz(I/O)(3.3V)	GND	51
48	CORE1(I/O)(1.8V)	REFCLK0	49
46	CORE2(I/O)(1.8V)	REFCLK0P	47
44	CORE3(O)(1.8V)	PERn0	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PETn0	37
36	UART K15 (I/O)(1.8V)	PETn0	35
34	UART K75 (I/O)(1.8V)	GND	33
32	UART TX (I/O)(1.8V)	GND	31
30	UART RX (I/O)(1.8V)	GND	29
28	UART RX (I/O)(1.8V)	GND	27
26	UART RX (I/O)(1.8V)	GND	25
24	UART RX (I/O)(1.8V)	GND	23
22	UART Rx (I/O)(1.8V)	SDIO Power0 (I/O)(1.8V)	23
20	UART Tx (I/O)(1.8V)	SDIO Wakeup (I/O)(1.8V)	21
18	GND	SDIO DATA0(O)(0.1V)	19
16	LED4 (I/O)	SDIO DATA2(O)(0.1V)	17
14	PCMC_OUT/DS_SD_OUT(O)(0.1V)	SDIO DATA7(O)(0.1V)	15
12	PCMC_IN/DS_SD_IN(O)(0.1V)	SDIO DATA7(O)(0.1V)	13
10	PCMC_SYNC/DS_WS(O)(0.1V)	SDIO CH0(O)(0.1V)	11
8	PCMC_CLK/DS_SCK(O)(0.1V)	SDIO CLK0(O)(0.1V)	9
6	LED4 (I/O)	GND	7
4	3.3V	USB_D+	5
2	3.3V	USB_D-	3
		GND	1

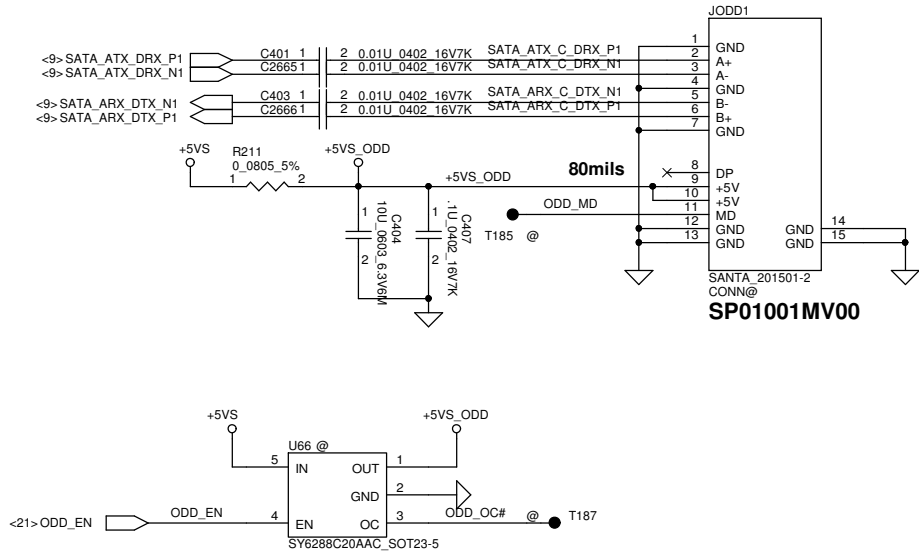


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Date: Thursday, February 26, 2015				Sheet	31 of 51

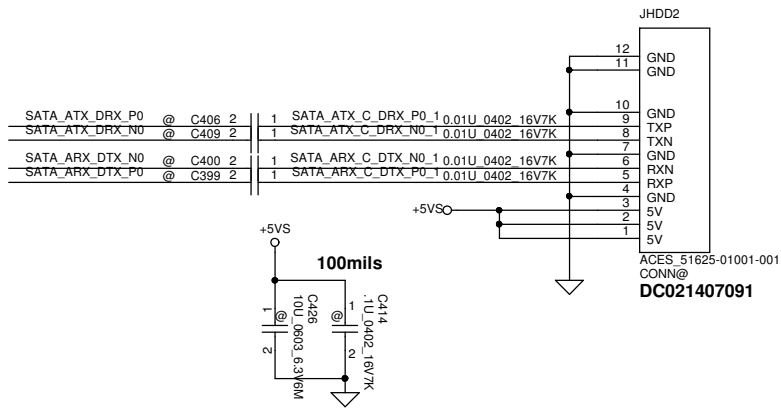
SATA HDD Conn.



SATA ODD Conn.

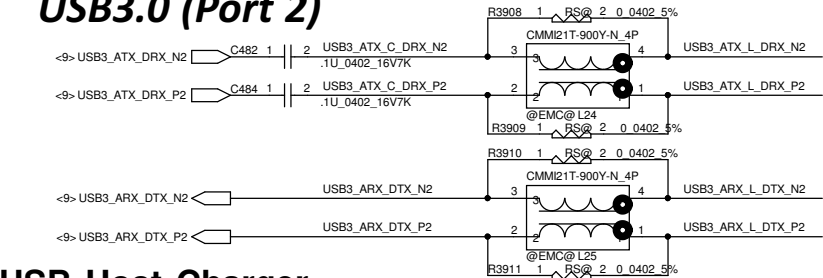


SATA HDD Conn.



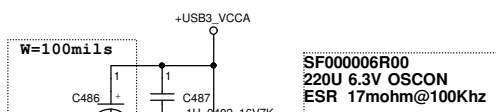
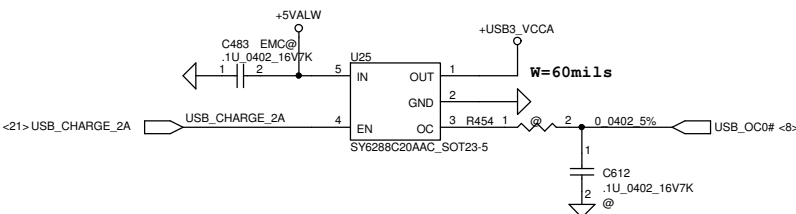
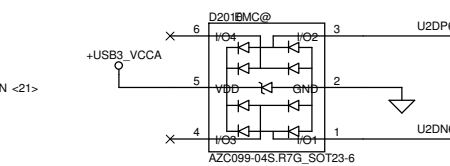
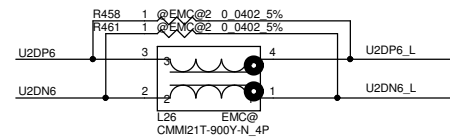
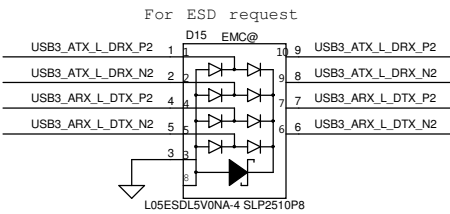
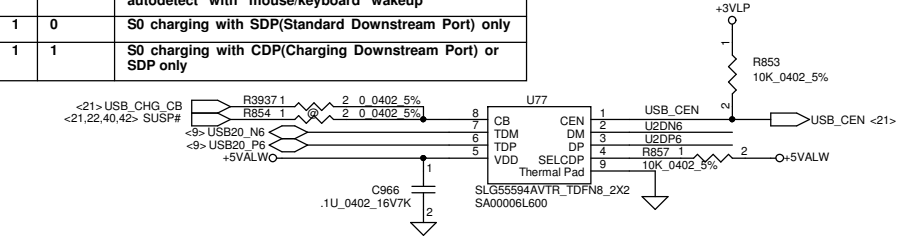
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Size		Document Number		Rev	
Custom		A4WAZ/A4WAR LA-C351P		1A	
Date:		Thursday, February 26, 2015		Sheet 32 of 51	

USB3.0 (Port 2)

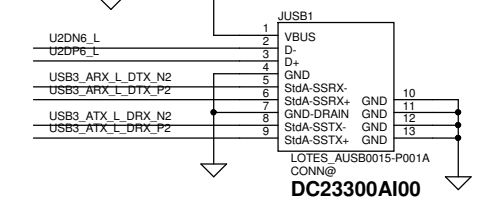


USB Host Charger

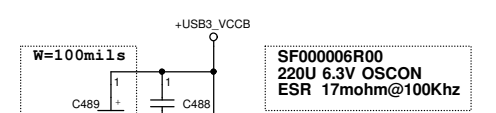
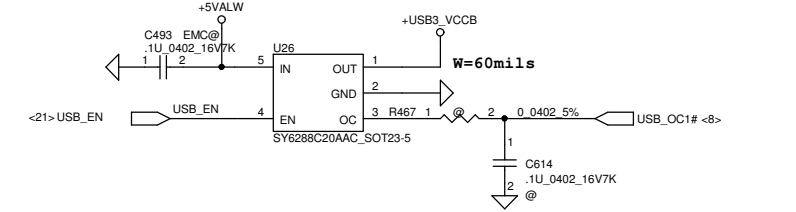
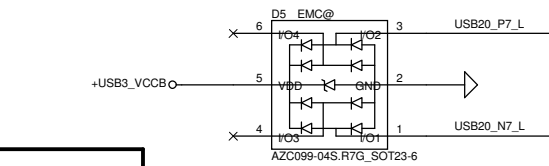
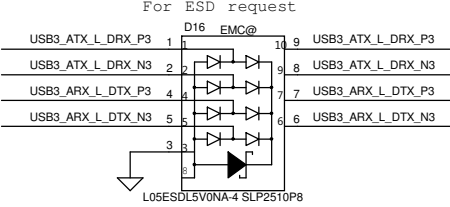
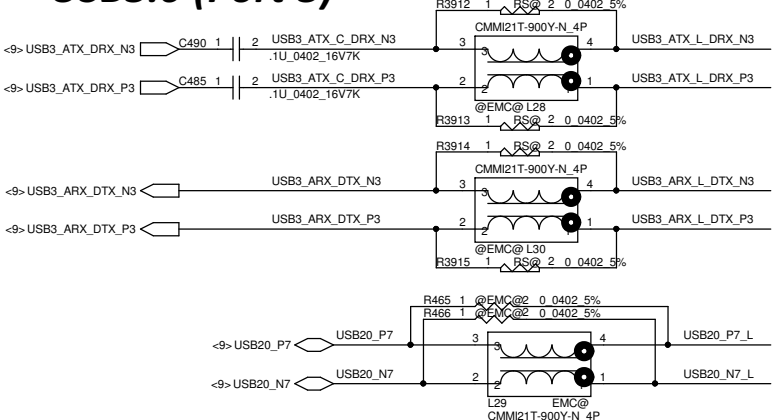
CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autotetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only



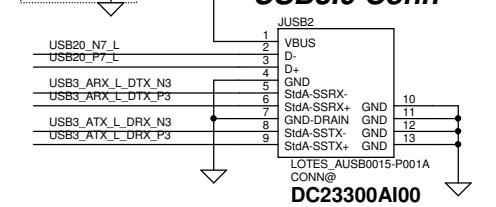
USB3.0 Conn.



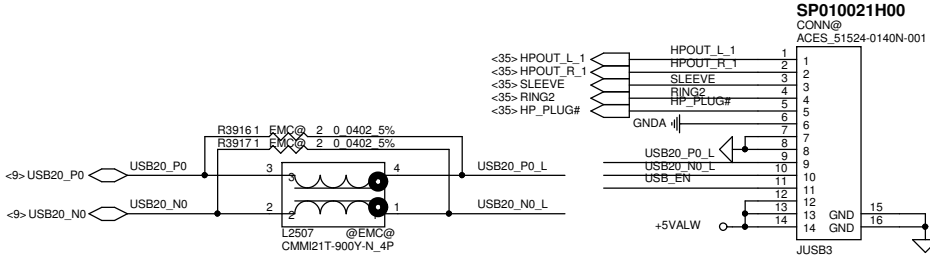
USB3.0 (Port 3)



USB3.0 Conn



USB/B (USB Port 3, + AUDIO)



The schematic shows the internal circuitry of the ON/OFF BTTN pin. It includes a pull-up resistor R534 (100K_0402_5%) connected to +3VLP0. The signal path goes through SW3 (EVQPLDA15 4P) to the test point BOT. The output is labeled <21> ON/OFFBTTN#.

Pin	Signal
27	ON/OFFBTTN#
26	KSO0
25	KSO1
24	KSO2
23	KSO3
22	KSO4
21	KSO5
20	KSO6
19	KSO7
18	KSO8
17	KSO9
16	KSO10
15	KSO11
14	KSO12
13	KSO13
12	KSO14
11	KSO15
10	KSO16
9	KSO17
8	KSI0
7	KSI1
6	KSI2
5	KSI3
4	KSI4
3	KSI5
2	KSI6
1	KSI7

ACES_85201-2805
CONN@

SP01000G000

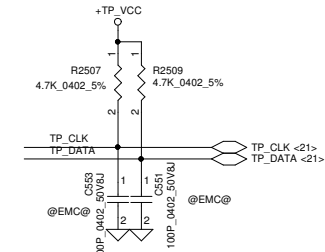
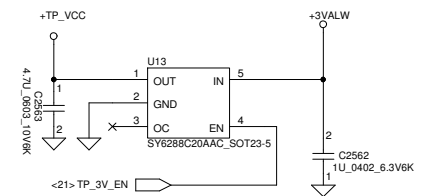
[illegible]

Diagram illustrating the connection of the ACES 5T524-0040N-001 connector (JBL1) to the microcontroller (U10: SV6288C20AAC_SOT23-5).

The microcontroller pins and their connections are:

- IN (1): Connected to +5V_S
- OUT (2): Connected to +5V_S
- EN (4): Connected to <21>KBL_EN through resistor R592 (0_0402_5%)
- OC (3): Connected to GND
- BL (5): Connected to a capacitor C524 (1_0402_16V7K) and then to the BL pin of the connector.

The connector (JBL1) pins and their connections are:

- Pin 1: Connected to GND
- Pin 2: Connected to GND
- Pin 3: Connected to GND
- Pin 4: Connected to GND
- Pin 5: Connected to BL
- Pin 6: Connected to GND

Additional components and labels include:

- Resistor R592 (0_0402_5%)
- Capacitor C524 (1_0402_16V7K)
- Microcontroller U10: SV6288C20AAC_SOT23-5
- Connector JBL1
- Power supply +5V_S
- Signal <21>KBL_EN
- Ground (GND)

GPIO3/BADD with Internal PH (default)

CLKRUN reserve PH 10K to +3VS at APU side

LPCPD# had internal PH

SERIRQ PH 10K to +3VS at PCH side

Pinmux diagram showing connections for NPC1650AA0WXX_TSSOP28 (SA000071000) to EMCC@.

Internal signals and pin connections:

- GPIO3/XOR_OUT (Pin 1)
- GPIO1 (Pin 2)
- GPIO2/GPX (Pin 3)
- GPIO3/BADD (Pin 4)
- GPIO4/CLKRUN# (Pin 5)
- LAD0/MISO (Pin 26)
- LAD1/MOSI (Pin 23)
- LAD2/SPI_IRQ# (Pin 20)
- LAD3 (Pin 17)
- LPCPD# (Pin 28)
- LPC_CLK1 (Pin 21)
- LPC_FRAME#_R (Pin 16)
- LPC_RST# (Pin 17)
- SERIRQ_R (Pin 7)
- VS_B (Pin 5)
- VDD (Pin 10)
- VDD (Pin 19)
- VDD (Pin 24)
- VDD (Pin 25)
- TEST (Pin 8)
- NC (Pin 3)
- NC (Pin 12)
- NC (Pin 13)
- NC (Pin 14)
- GND (Pin 4)
- GND (Pin 11)
- GND (Pin 18)
- GND (Pin 25)

Package: NPC1650AA0WXX_TSSOP28
SA000071000
TMP@

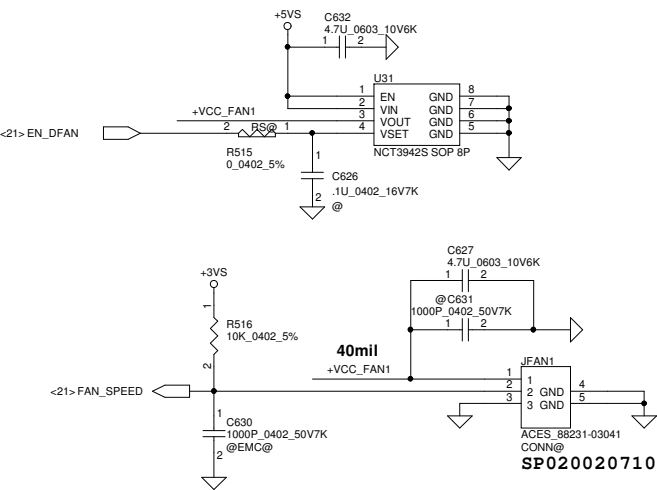
Connections to EMCC@:

- LPC_CLK1 (R2603)
- R2603
- 33 0402 5%
- C2606 1
- 22P 0402 50V8J

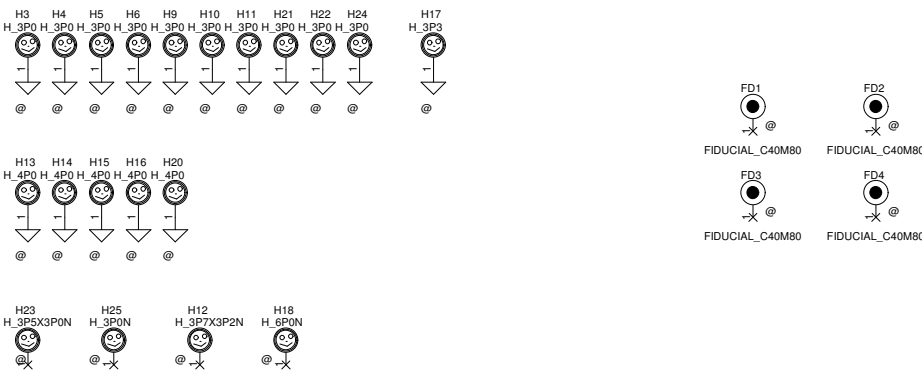
Pin 1-12 connection diagram for the SP01001FR00 module. The diagram shows a 12-pin connector with pins 1-10 labeled 1 through 10, and pins 11 and 12 labeled GND1 and GND2 respectively. Pin 1 is connected to +3VLP. Pin 2 is connected to LID_SW2#. Pin 3 is connected to SEN_DET#. Pin 4 is connected to BATT_AMP_LED#. Pin 5 is connected to BATT_BLUE_LED#. Pin 6 is connected to PWR_SUSP_LED#. Pin 7 is connected to PWR_LED#. Pin 8 is connected to +3VALW. Pin 9 is connected to GND1. Pin 10 is connected to GND2. The diagram also shows a 3VLP supply and a 3VALW supply. The module is identified as SP01001FR00.

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				Size	Document	Number		Rev	IA
				Custom		A4WAZ/A4WAR LA-C351P			
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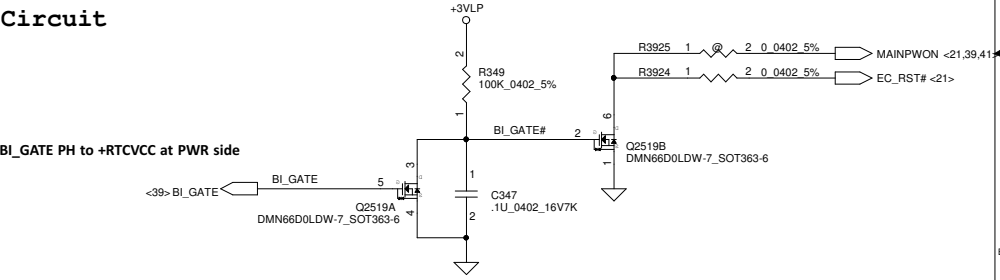
FAN1 Conn



Screw Hole

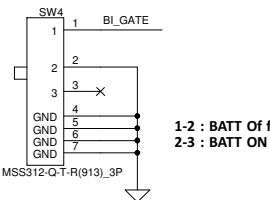
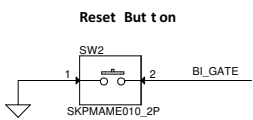


Reset Circuit



Debug SW

Reset But t on



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- 0.1
1. Change R3880 to 0603 0ohm
 2. Change R346 to 22Kohm
 3. Unpop RV163,RV81,RV82,RV83
 4. Unpop R1691,R1692,R1693,R1694

- 0.2
1. Pop RV160,RV161 for Exo
 2. Pop C543 for HDMI DDC electrical test
 3. Pop R81;change R2626 to 4.22K for HDMI EA
 4. Add CV2698 at VGA_ON
 5. JUSB3 pin reverse
 6. C794,C795 change to 5.6P;C682 change to 22P
 7. Unpop CV11
 8. Pop R1562;R1564 15K for CZ, 20K for CZL
 9. Remove MIC1,D58,R460
 10. Combine power
 11. Add R3922,R3923
 12. Change SW4 footprint
 13. Change R1,R3 to 470ohm
 14. Change L2506 to SH00000RT00
 15. Combine power
 16. Add R3924,R3926;reserve R3925,D2012,D2013,D2014
 17. Change L2503,L2504,L2505 to SM01000LU00
 18. Combine power
 19. Reserve R3927
 20. Combine power
 21. Add R3928,R3929,R3931; reserve R3930
 22. Change R3890,R3891 to 10K
 23. Change R349 to 100K
 24. Change R2 to 562ohm
 25. Unpop R3922,R3923,Q2505,Q87

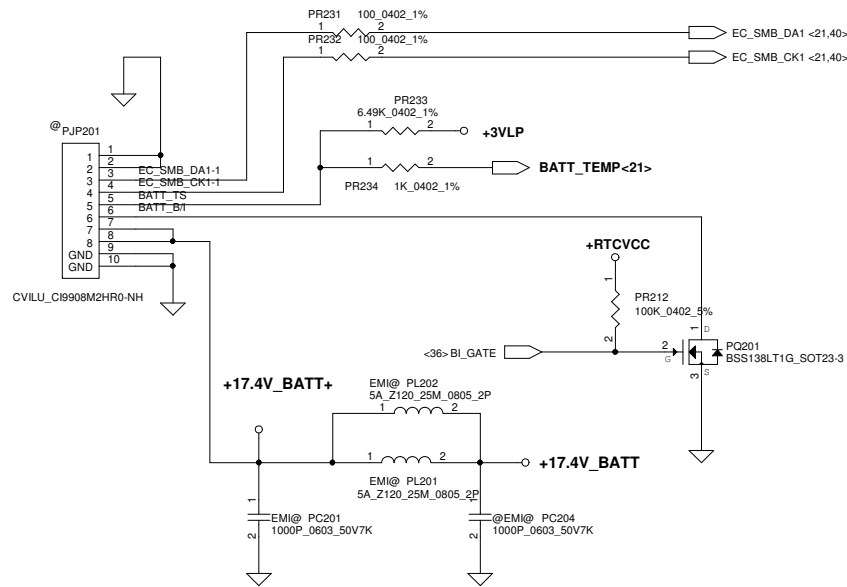
- 1.0
1. Unpop R3931, add R3934
 2. Change R1,R3 to 560ohm; R2,R6 to 430ohm
 3. Change H17 to H_3P3
 4. Unpop U2606; pop R212
 5. Add R3935, unpop U2504
 6. RP26 1K for CZL; 2.2K for CZ
 7. Reserve R3936
 8. Pop R211; unpop U66
 9. Unpop R682,R694,R704,R705,R706,R707,R708
 10. Change R1690,RV1630,RV1631,RV27,RV30,RV31,R119,R157,R456,R464,R470,R471,R472,R854,R1682,R3824,R3834,R3849,R16,R3902,R3903 to R-Short
 11. Change R2140 to 27K
 12. Combine power
 13. Change R106,R756,R765,R769,R779,R781,R782,R783,R794,R3908,R3909,R3910,R3911,R3912,R3913,R3914,R3915,R427,R428 to R-Short
 14. R107 22ohm for CZL; 0ohm for CZ
 15. Change C2647,C2648 to 6.8p
 16. Change C644 to 330u
 17. Change R854 to 0ohm unpop; add R3937
 18. Combine power
 19. R1564 27k for CZ; 33k for CZL
 20. Add R3932 for dGPU, reserve R3933,U2612
 21. Combine power
 22. Pop U69 use memo control
 23. Change L26, L69 to SM070002J00
 24. Change R3903,R3902 to 0ohm pop
 25. Change U2608 to SA000088800; R3902,R3903 to 1Kohm; unpop R3890,R3891
 26. Change U2608 to SA003930080; R3902,R3903 to 0ohm; R3890,R3891 to 1Kohm pop
 27. Change U2608 to SA000088800; R3902,R3903 to 1Kohm; unpop R3890,R3891

- 1A
1. Change R872 to 0ohm unpop; R873 to 0ohm pop
 2. R1564 43k for CZ; 56k for CZL
 3. Combine power
 4. Reserve R3938,R3939
 5. Reserve R3940

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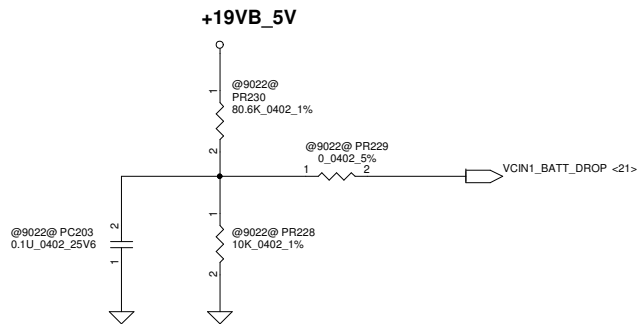


---Battery_pin define---
 PIN1 GND
 PIN2 GND
 PIN3 SMD
 PIN4 SMC
 PIN5 TS
 PIN6 B/I
 PIN7 Batt+
 PIN8 Batt+

---Battery Con_pin define---
 PIN8 GND
 PIN7 GND
 PIN6 SMD
 PIN5 SMC
 PIN4 TS
 PIN3 B/I
 PIN2 Batt+
 PIN1 Batt+

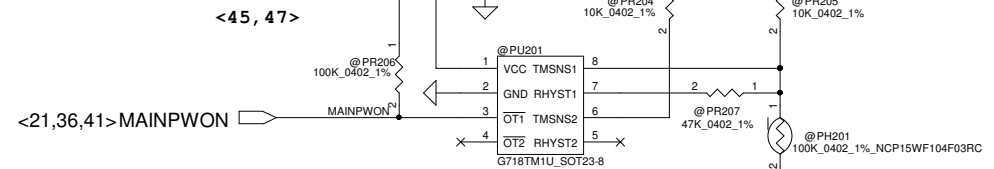
2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Reserve for 2-cell design



For 45W adapter==>action 48.15W , Recovery 38.7W
 48.15W:
 $I_{ada} = 0 \sim 2.253A$ ($48.15W/19V=2.534A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 2.534 * 0.02 = 1.01$
 38.7W:
 $I_{ada} = 0 \sim 2.036A$ ($38.7W/19V=2.036A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 2.036 * 0.02 = 0.814$
 $CP = 45W * 0.85 = 38.25W$

For 65W adapter==>action 69.55W , Recovery 55.9W
 69.55W:
 $I_{ada} = 0 \sim 3.661A$ ($69.55W/19V=3.661A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 3.661 * 0.02 = 1.464$
 55.9W:
 $I_{ada} = 0 \sim 2.942A$ ($55.9W/19V=2.942A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 2.942 * 0.02 = 1.177$
 $CP = 65W * 0.85 = 55.25W$

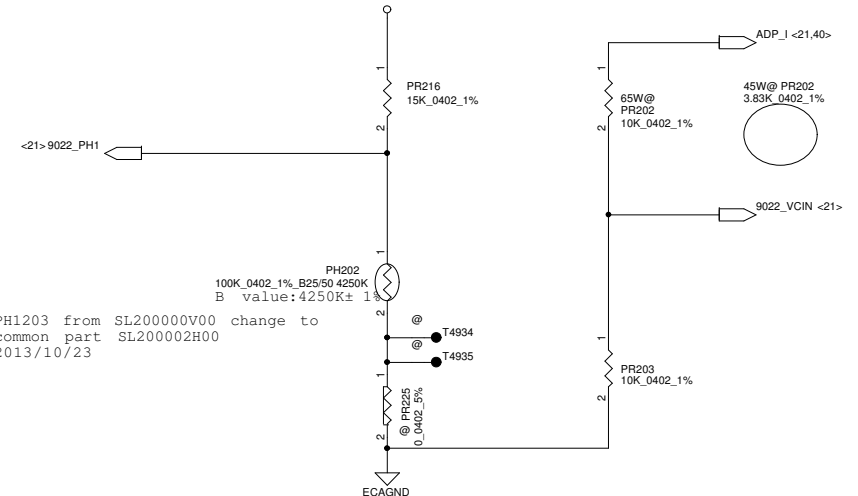


2013/10/28 update PH201 chang
Common part SL200002H00

For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	92C, 1V	56C, 2V
PH202 (ohm)	7.3K	26.11K

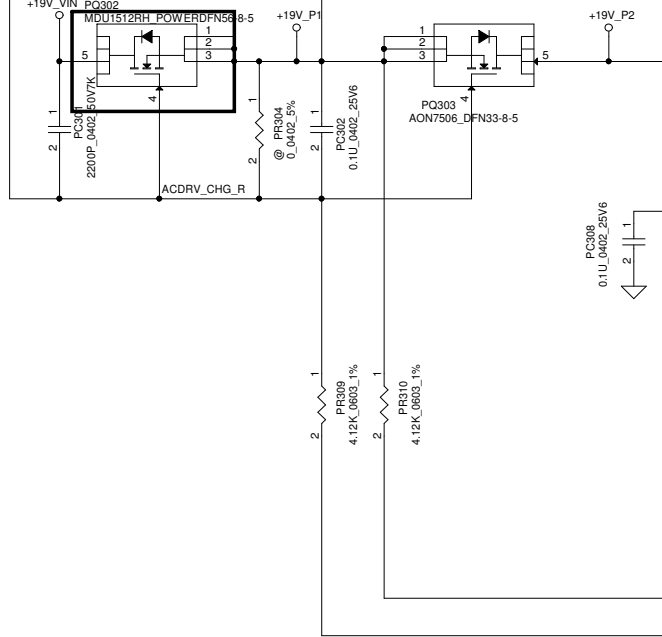
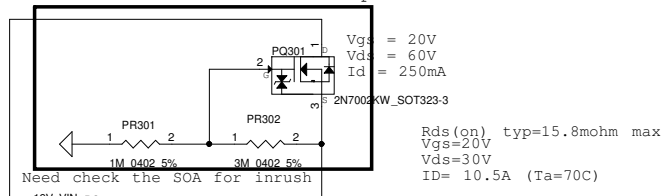
For KB9012 sense 20mΩ	Active	Recovery
45W	48.15W, 0.73V	38.7W, 0.59V
65W	69.55W, 0.73V	55.9W, 0.59V

PH202 under CPU bottom side :
 CPU thermal protection at 92 degree C (shutdown)
 Recovery at 56 degree C +EC_VCCA

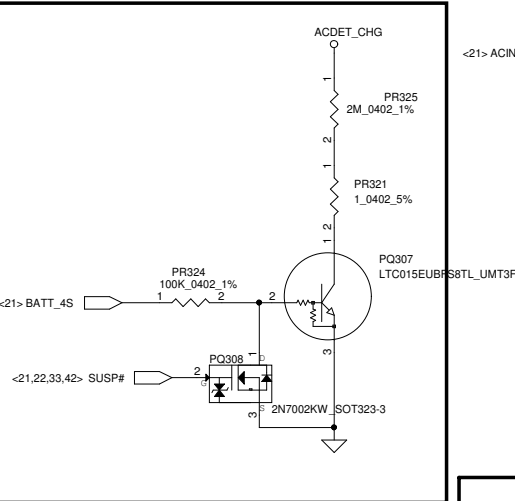


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								BATTERY CONN / OTP			
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Protection for reverse input

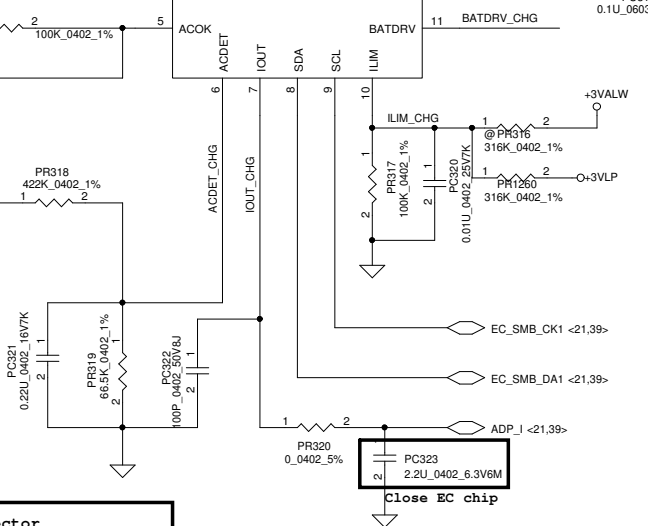


For 4S per cell 4.35V battery



Vin Detector			
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+316)/20/0.01
= 3.96 A



****Design Notes****

#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W.

#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke

#Circuit Design
1. ACOK,ILIM pull high voltage need base on 3/5V enable control
2. Use 10X10 choke and 3X3 H/L Side MOSFET

Charge current 3.5A
Power loss : 1.82W
Power density : 0.81 (15X15)

3. If use 4S per cell 4.35V battery, need additional circuit for ACDET(PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)
4. PC223 0.22uF can't be changed. (Wrong adapter concern)
5. For the design, need double confirm PQ202,PQ203,PQ204 rating

#Protect function
1. AC0VP : ACDET voltage > 3.14V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOC : 3/4.5/6A based on current current setting
5. BATLOVP : 103-106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 150mV (default)

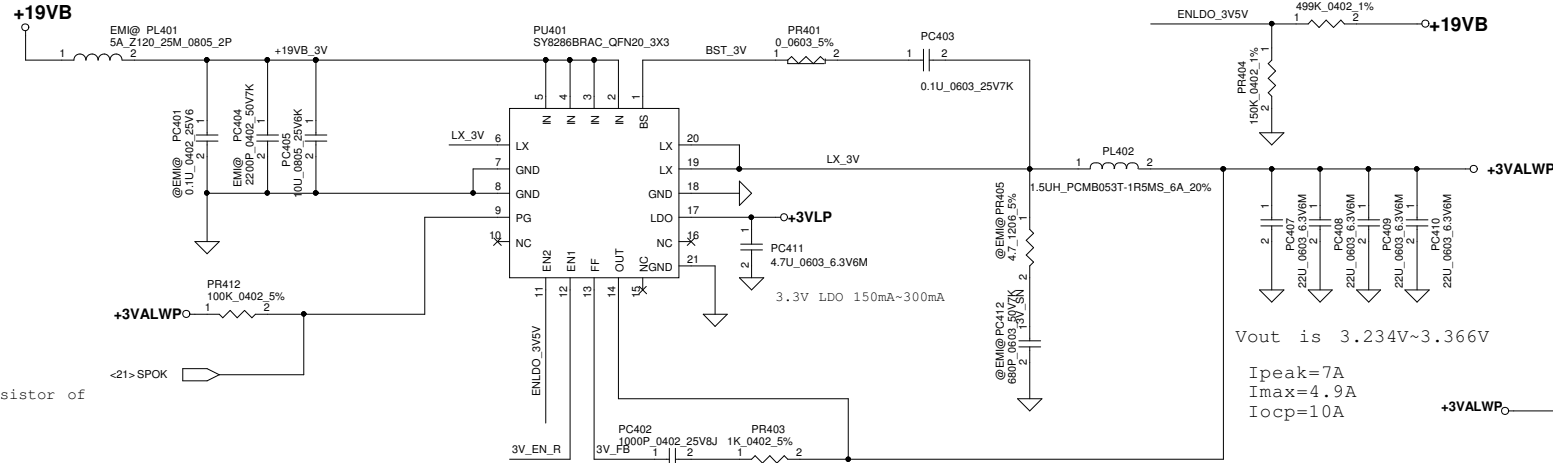
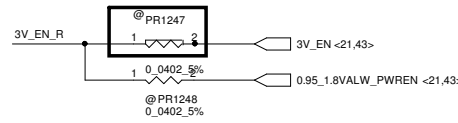
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2015/02/25				Title			
Deciphered Date				2017/02/25				CHARGER			
Size				Document Number				Rev			
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Module model information

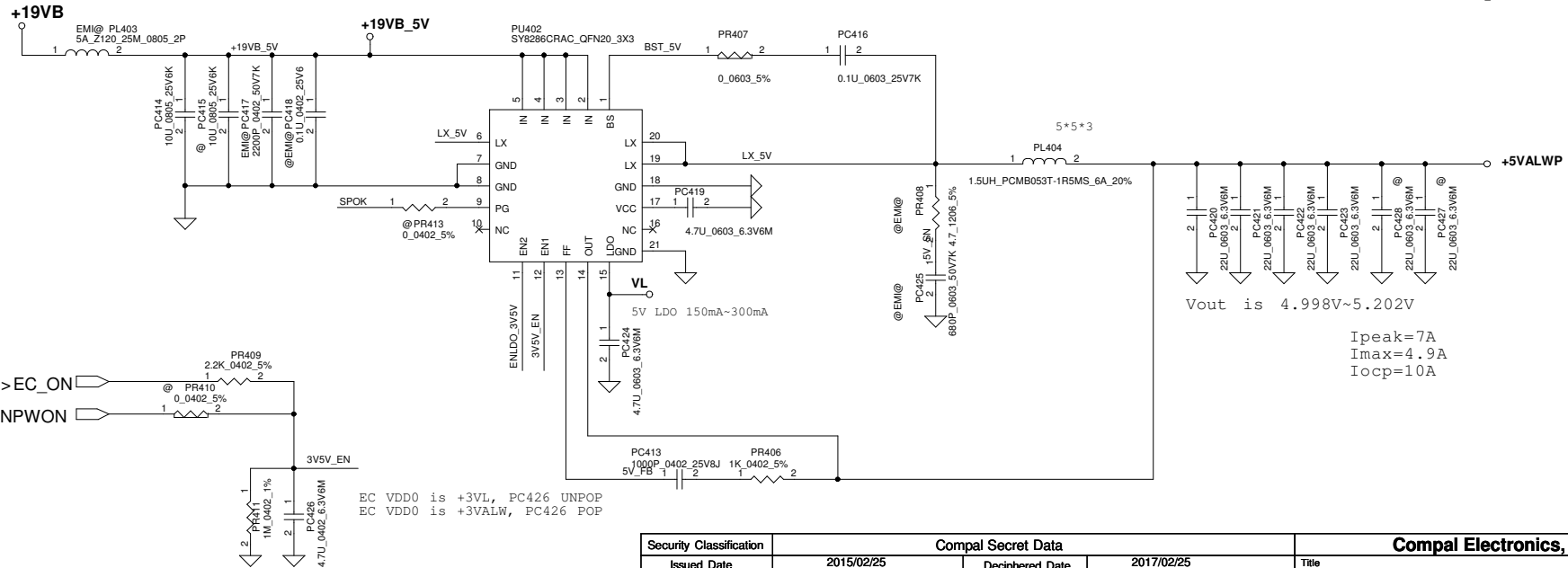
SY8208B_V2.mdd

SY8208C_V2.mdd



+3VALWP

+5VALWP



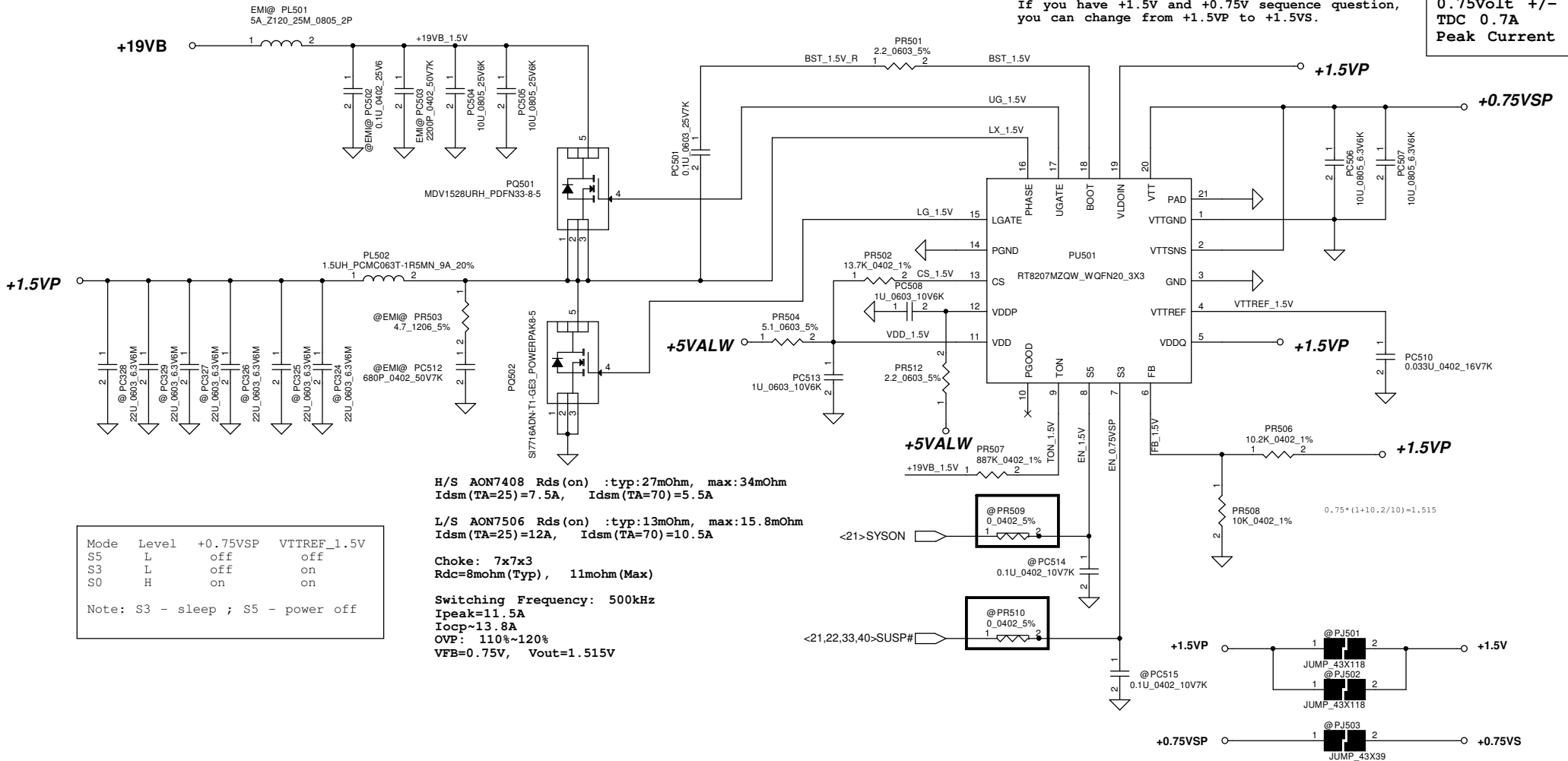
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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

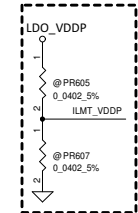
0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



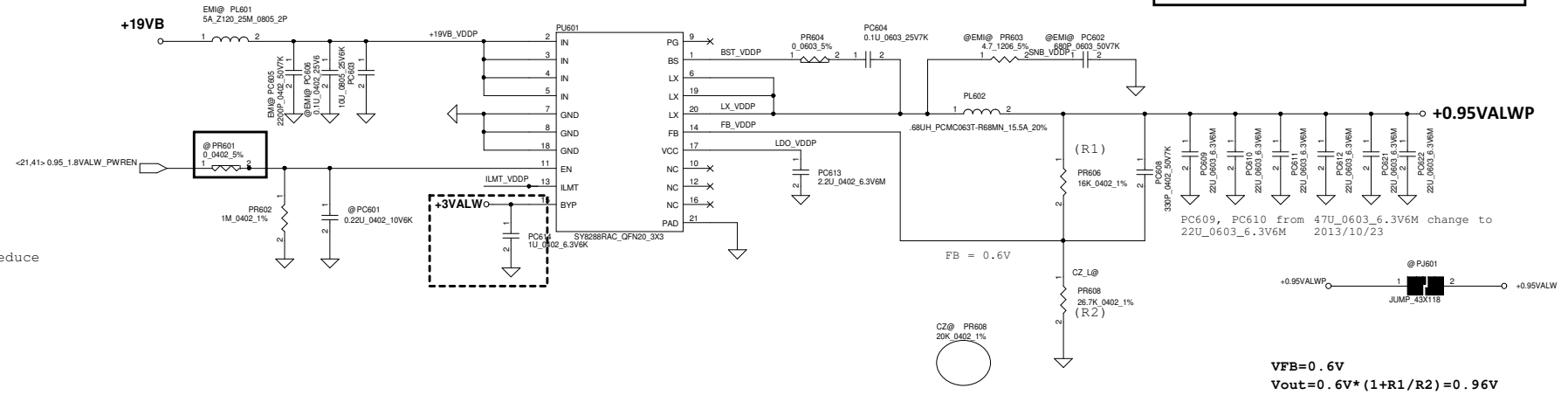
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EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

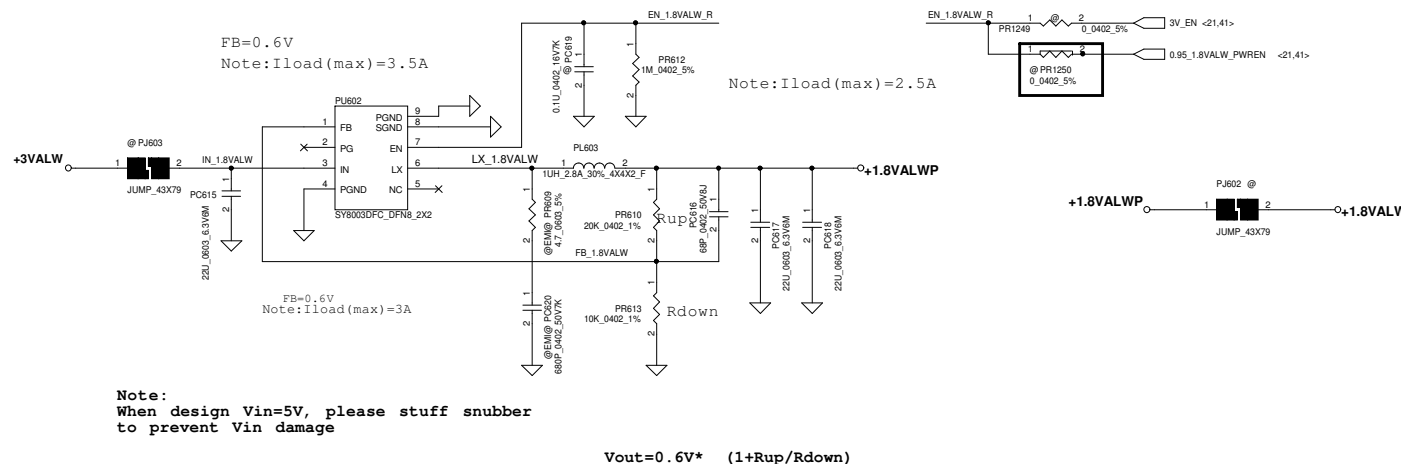
Module model information
SY8208D_V1.mdd



PR606 part count reduce



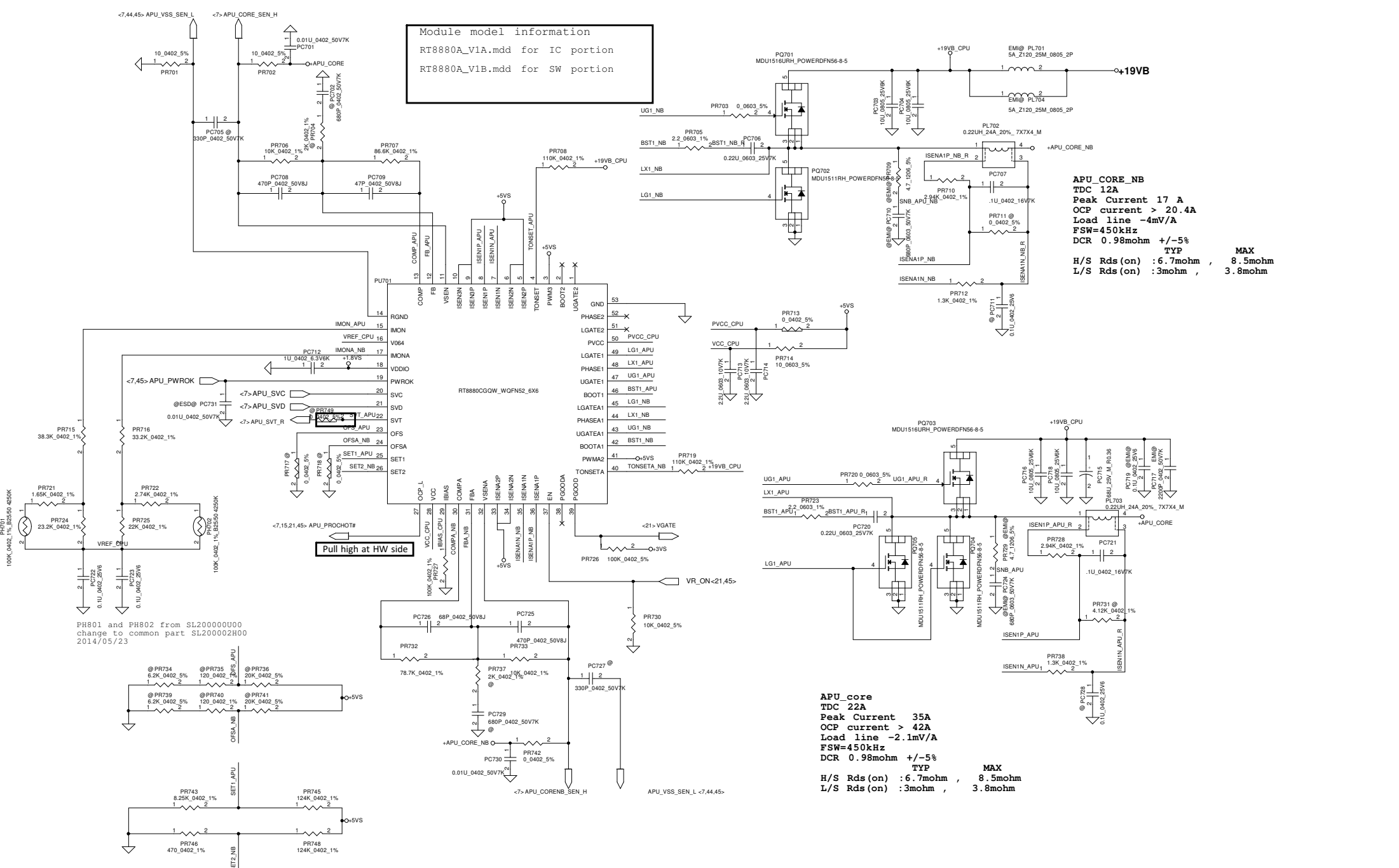
$V_{FB} = 0.6V$
 $V_{out} = 0.6V * (1 + R1/R2) = 0.96V$



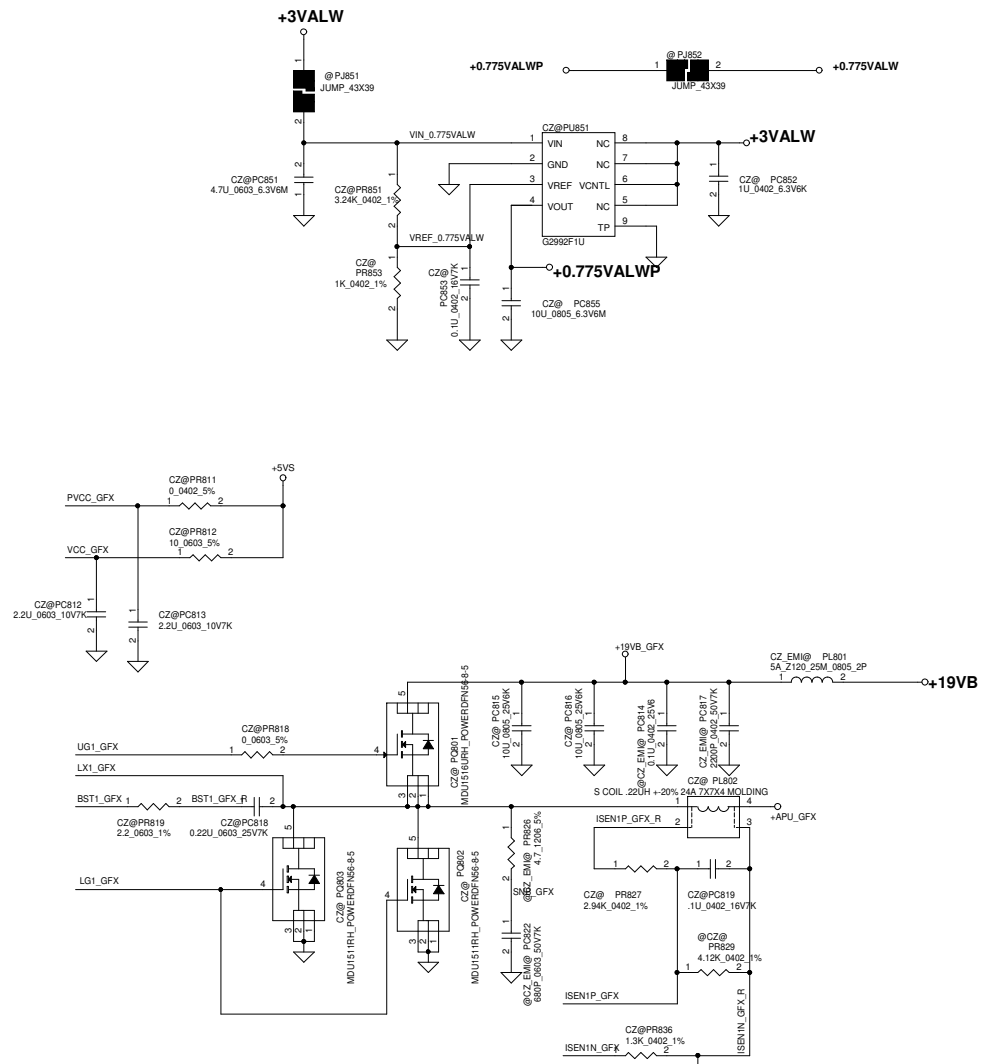
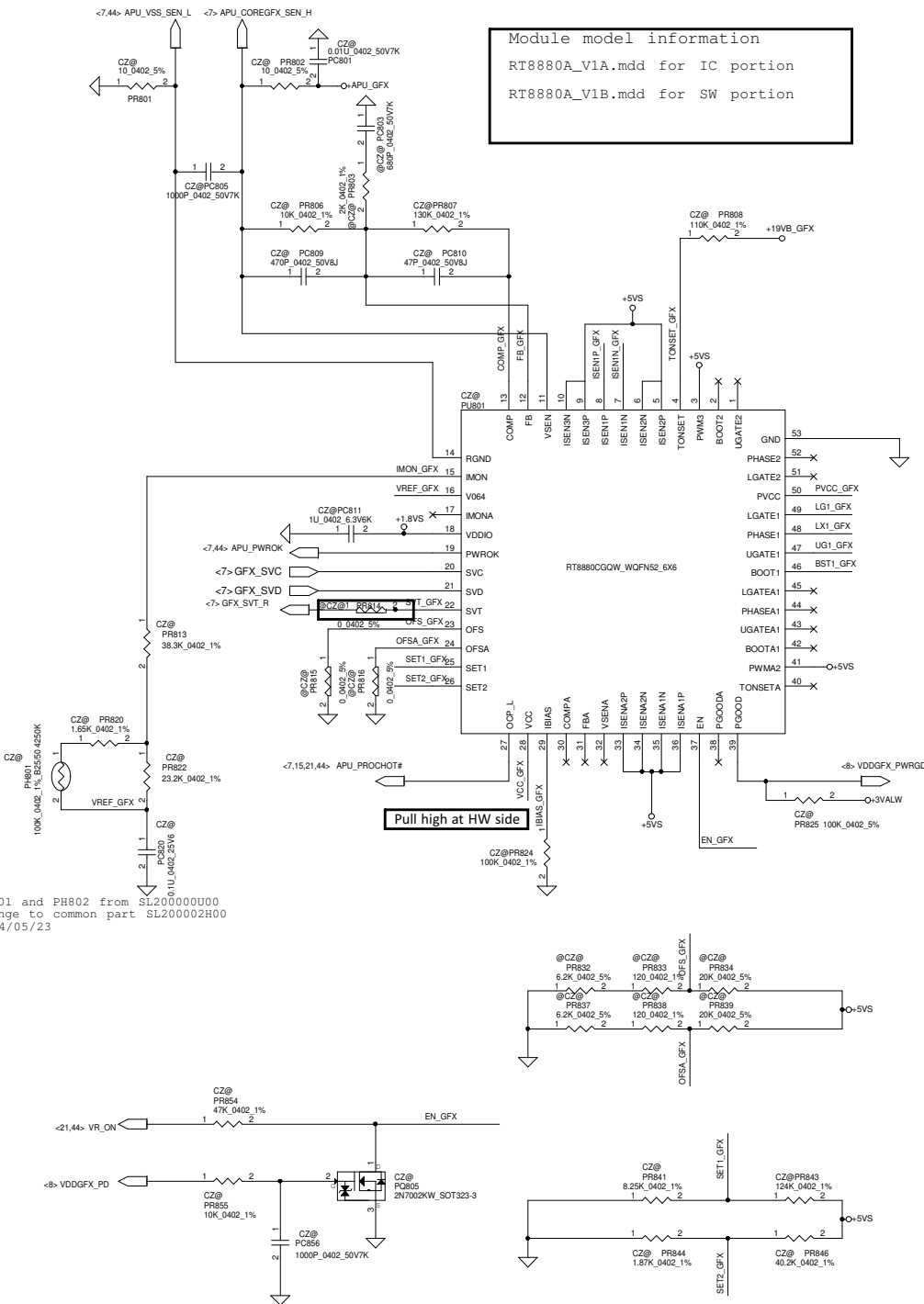
Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

$V_{out} = 0.6V * (1 + R_{up}/R_{down})$

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GFX_core
TDC 22A
Peak Current 35A
OCF current > 42A
Load line -2.1mV/A
FSW=450kHz
DCR 0.98mohm +/-5%
H/S Rds(on) : 6.7mohm , 8.5mohm
L/S Rds(on) : 3mohm , 3.8mohm

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+APU_CORE

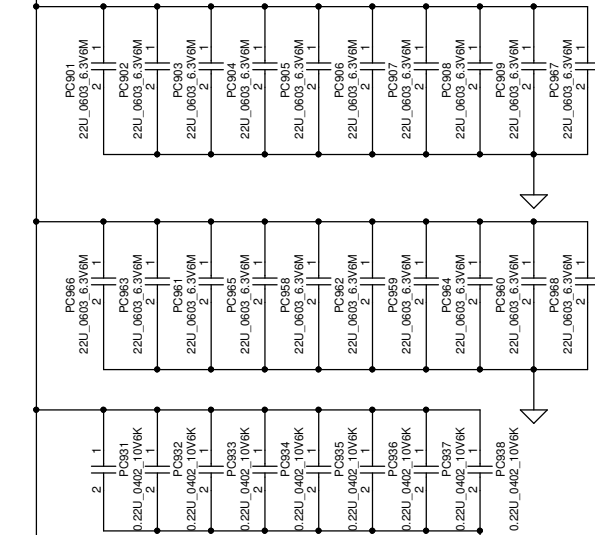
+APU_CORE_NB

+APU_GFX

+APU_CORE

+APU_CORE_NB

+APU_GFX

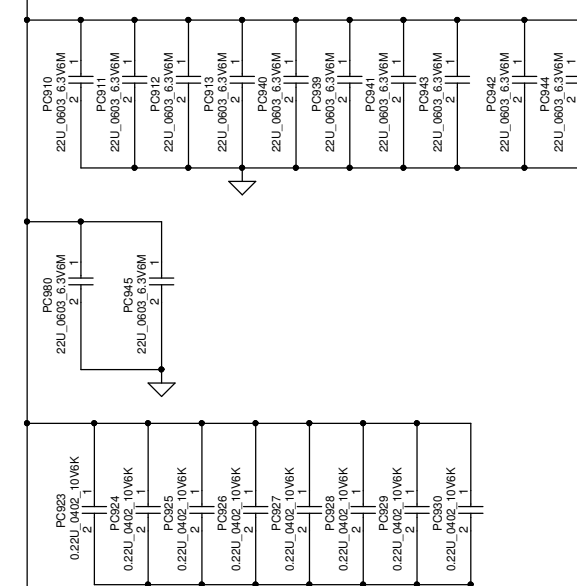
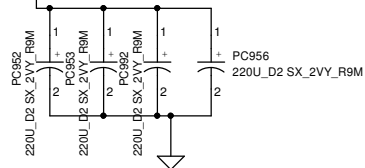


APU_CORE

220uF*4
22uF*20+0.22uF*8
+180pF*1

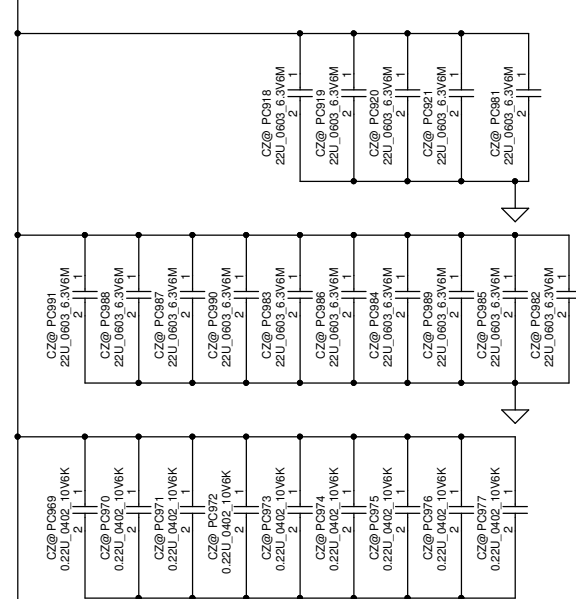
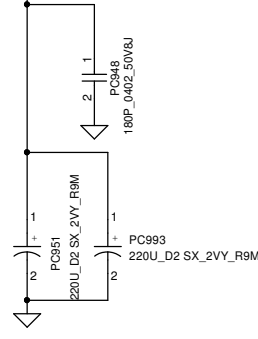
under 22u*9
 0.22u*8
 near 180p*1

+APU_CORE



APU_CORENB
220uF*2
22uF*12+0.22uF*8
180pF*1

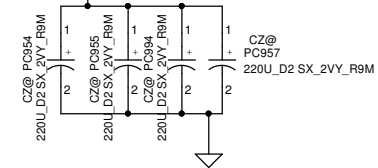
under 22u*4
 0.22u*8
 near 180p*1



APU_GFX
330uF*1
220uF*3
22uF*15+0.22uF*9
+180pF*1

under 22u*9
 0.22u*9
 near 180p*1

+APU_GFX



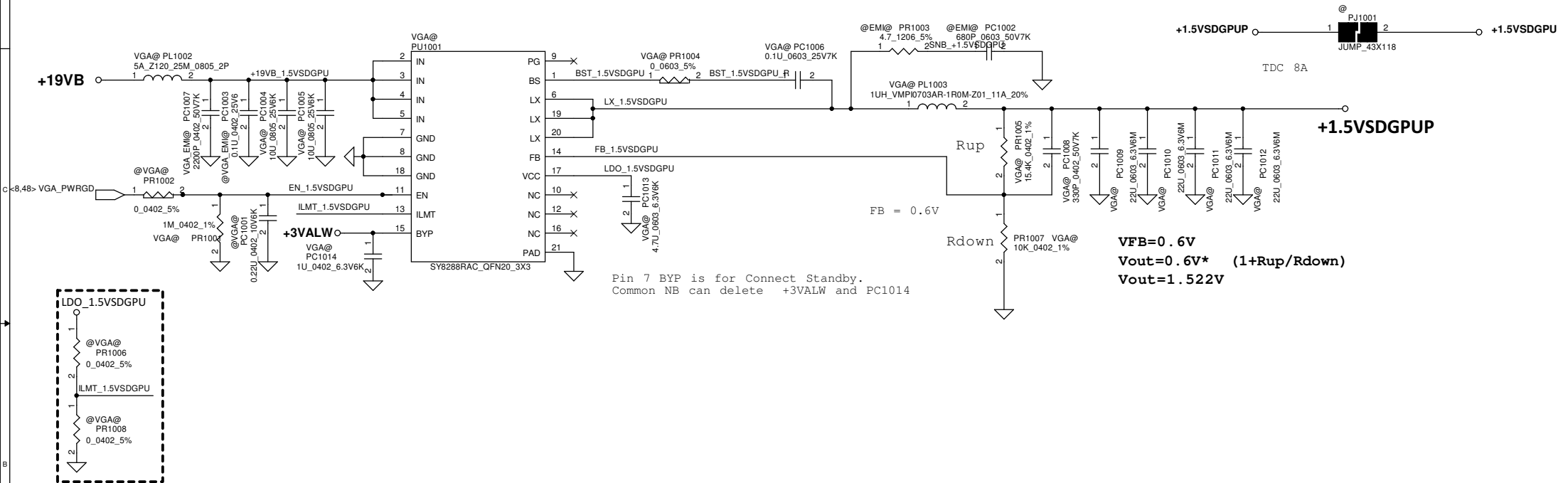
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						Size		Document Number		Rev 1A	
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Module model information

SY8208D_V1.mdd

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

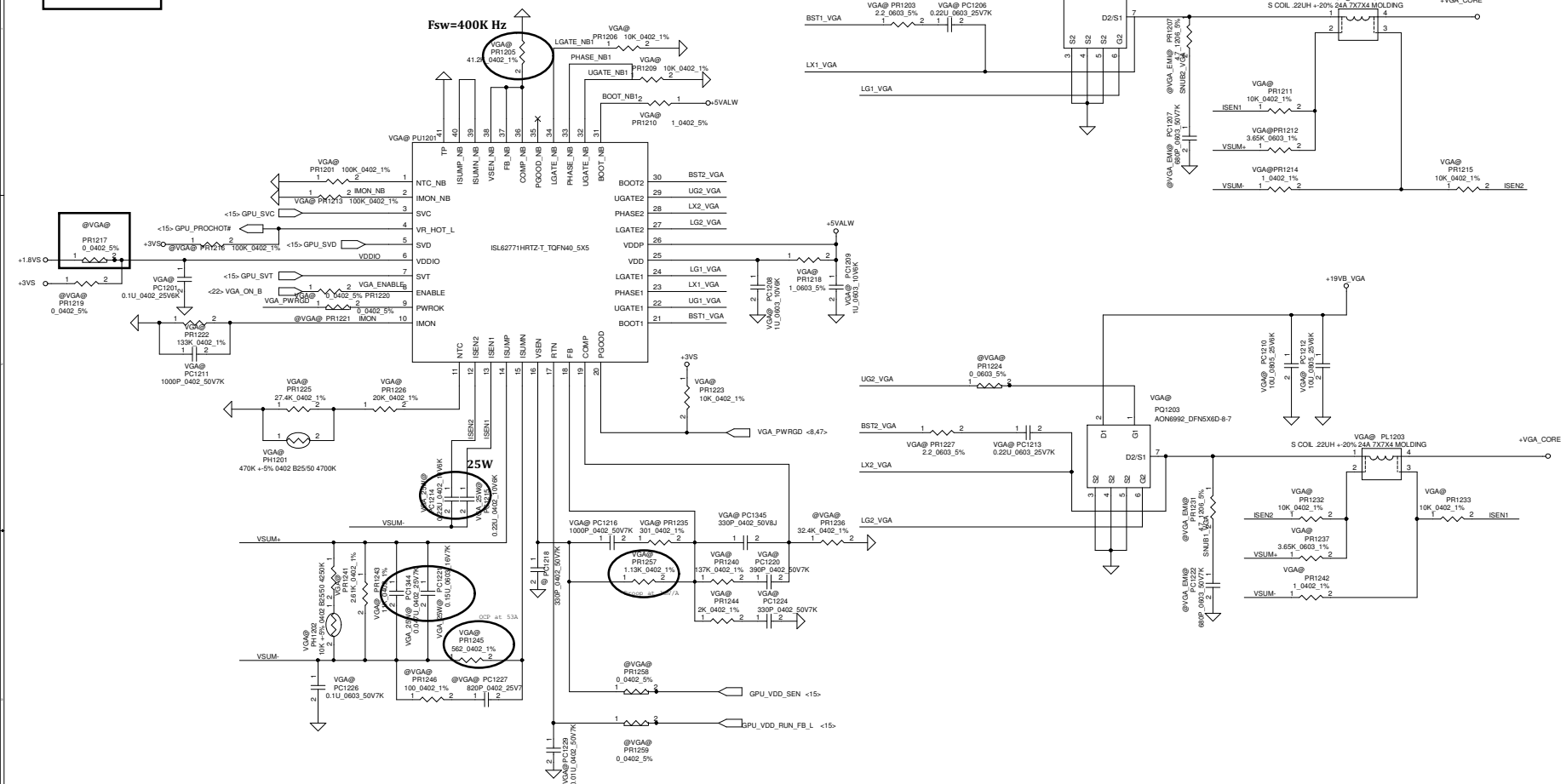
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



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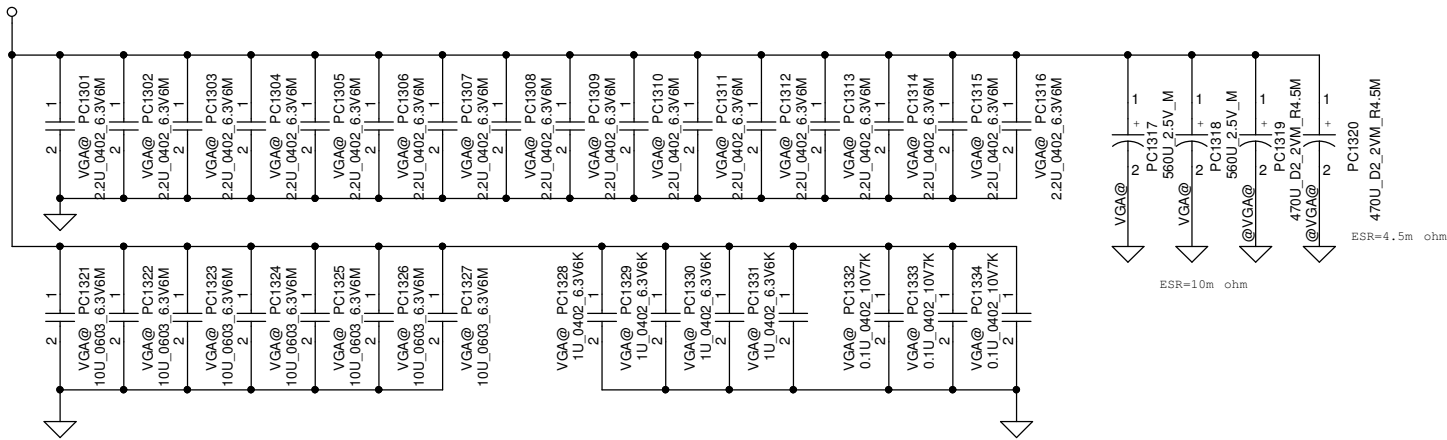
+VGA_CORE
AMD TOPAZ
TDC 31A, EDC 46.5A
OCP min 58.1A

AMD JET LE
TDC 20A, EDC 30A
OCP min 37.5A



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+VGA_CORE



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				VGA_CORE CAP	
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01				P39	PC204 change to non-pop		
02	for pop list			P45	PR811 change to pop		EVT
03				P46	PC956 change to 220U CZ@ PC957 change to 220U		
04				P48	PQ1201 and PQ1203 AON6970 change to AON6992		EVT
05		change 3V/5V/0.95V/1.5VDGPU IC			PU401 change to SY8286BRAC_QFN20_3X3 PU402 change to SY8286CRAC_QFN20_3X3 PU601 and PU1001 change to SY8288RAC_QFN20_3X3		EVT
06	add and delete pop list				PR316 change to no-pop PR1260 change to pop PR749 change to pop PL301 change to pop PR604 change to pop PR216 Change 15k		DVT
07	Change part list				PQ201 Change to SB00000QO00 PR401 change to 0 ohm PC402 change to SE068102J80 PR407 change to 0 ohm PC413 changet to SE068102J80 PL101,PL201,PL202,PL401,PL403,PL501,PL601, PL701,PL704,PL801,PL1002,PL1202 change to common part PL402 ,PL404,PL502 change to common part PR606 change to 16K PR608 change to 26.7K PL1003 change to common part delt PR614 and PR852 PU851 change to SA00000VE80 det PR1255 det PC607		DVT
08					1. PR321 change to 1 ohm 2. PR1247,PR509,PR510,PR601,PR1250,PR749,PR814, PR1217 change to R-short 3. PC328,PC329,PC327,PC326,PC325,PC324 change to un-pop 4. PU501 change to RT8207M 5. PR507 change to 887k 6. PR722 change to 2.74k 7. PR748 change to 36k 8. PR746 change to 3.3k 9. PR707 change to 86.6k 10. PC709 change to 47p 11. PC810 change to 47p 12. PC805 change to 1000p 13. PR807 change to 130k 14. PR846 change to 40.2k 15. PR844 change to 1.87k 16. PQ701, PQ703 ,PQ801 change to SB00000S800 17. PQ702,PQ704,PQ705,PQ802,PQ803 change to SB00000SD00 18. PQ306 change to SB00000V100 19. PQ305, PQ501 change to SB00000S500 20. PQ502 change to SB00000GW00 21. PQ1201 change to SB000017L00 22. PR748 SD034124380 23. PR746 SD034470080 24. PC323 change to pop		PVT

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				PWR_PIR1
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01					PR320 change to 0 ohm PR401, PR407, PR604, PR713, PR1004 change to R-short		PR-MP
03							
04							
05							
06							
07							
08							